PICMG 2.0 R2.1

CompactPCI™ Specification

June 17, 1997

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1. Overview

1.1 CompactPCI Objectives

CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification* 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. CompactPCI uses industry standard mechanical components and high performance connector technologies to provide an optimized system intended for rugged applications. CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

CompactPCI is an open specification supported by the PICMG (PCI Industrial Computer Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications. PICMG controls this specification.

1.2 Background and Terminology

Eurocard - A series of mechanical board form factor sizes for rack-based systems as used in VME, Multibus II, and other applications defined by the Institute of Electrical and Electronics Engineers (IEEE) and International Electrotechnical Committee (IEC).

ISA - Industry Standard Architecture. A specification by which Personal Computers (PCs) add boards.

PCI - Peripheral Component Interconnect. A specification for defining a common interconnect between logic components. Typically used for interconnecting high-speed, PC-compatible chipset components. The PCI specification is issued through the PCI Special Interest Group (PCI SIG).

This specification utilizes several key words, which are defined below:

may: A key word indicating flexibility of choice with no implied preference.

shall: A key word indicating a mandatory requirement. Designers **shall** implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.

should: A key word indicating flexibility of choice with a strongly preferred implementation.

1.3 Desired Audience

CompactPCI exists to provide a standard form factor for those applications requiring the high performance of PCI as well as the small size and ruggedness of a rack mount system. CompactPCI provides a mechanism for OEM and end users to directly apply PCI components and technology to a new mechanical form factor while

maintaining compatibility with existing operating systems and application software available for desktop PCI.

A CompactPCI system **may** form the high performance core of a system that utilizes a legacy bus, such as ISA, STD 80, STD 32 or VME, for expansion I/O and other functions.

1.4 CompactPCI Features

CompactPCI appeals to customers that require the following capabilities:

- 33 MHz PCI performance
- 32- and 64-bit data transfers
- 8 PCI slots per bus segment
- Industry standard software support
- 3U small form factor (100 mm by 160 mm)
- 6U form factor (233.35 mm by 160 mm)
- IEEE (1101.1, 1101.10 and P1101.11) Eurocard packaging
- Wide variety of available I/O

1.5 Applicable Documents

This *CompactPCI Specification* builds on several industry standards. You should reference the following list of publications while reading this specification.

- *PCI Local Bus Specification*, PCI Special Interest Group, 5200 N. E. Elam Young Parkway, Hillsboro, Oregon, USA, 9724-6497, (503) 696-2000
- IEC 297-3 and -4, *Eurocard Specification*, Bureau Central de la Commission Electrotechnique Internationale, 1 rue de Varembe, Geneva, Switzerland, 011.412.291.90228
- IEC-1076-4-101, *Draft Specification for 2 mm Connector Systems*, International Electrotechnical Commission, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY, USA 10036
- IEEE 1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*, Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331
- IEEE 1101.10, *IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice*, Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331
- IEEE P1101.11, *IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice*, Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331

1.6 Administration

CompactPCI is an open specification supported by the PCI Industrial Manufacturers Group (PICMG). PICMG maintains this specification and is chartered to:

- Extend the PCI standard into industrial systems
- Manage and maintain relevant PCI specifications
- Contribute to the establishment of relevant PCI specifications as an industry wide specification

For information on how to become a PICMG member, please contact:

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The PCI Industrial Computer Manufacturers Group's policy regarding the use of the trademarks, *PICMG, CompactPCI,* and the *PICMG, CompactPCI* logos is as follows:

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- Permission to use the PICMG and CompactPCI logo is automatically granted to designated members only as stipulated on the most recent *Membership Privileges* document, during the period of time for which their membership dues are paid.
- Member's distributors and sales representatives **may** use the *PICMG* and *CompactPCI logo* in promoting member's products sold under the name of the member.
- The PICMG and CompactPCI logos **shall** be printed in black or in color as illustrated on the Logo Page that is available from the PICMG at the address above. The center bar of the logo containing the phrase "PICMG" or "CompactPCI" is set horizontally and the aspect ratio of the logo **shall** be maintained, but the size may be varied. Nothing may be added to or deleted from the *PICMG* and *CompactPCI* logos.
- Since the *PICMG* and *CompactPCI* logos, and the *PICMG* and *CompactPCI* names are trademarks of the PICMG, the following statement **shall** be included in all published literature and advertising material in which the logo appears:

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2. Feature Set

2.1 Form Factor

The form factor defined for CompactPCI boards is based on the Eurocard industry standard. Both 3U (100 mm by 160 mm) and 6U (233.35 mm by 160 mm) board sizes are defined. Figure 1 shows a 3U style board.

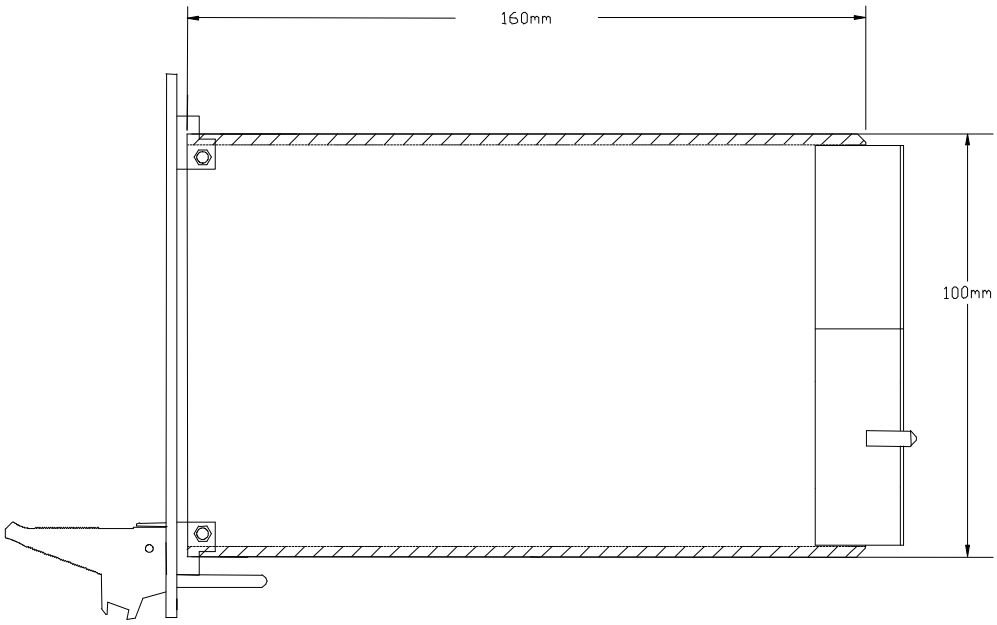


Figure 1. 3U 64-Bit CompactPCI Form Factor.

A CompactPCI system is composed of one or more CompactPCI bus segments. Each segment is composed of up to eight CompactPCI slots (at 33 MHz) with 20.32 mm (0.8 inch) board center-to-center spacing. Each CompactPCI bus segment consists of one System Slot, and up to seven Peripheral Slots.

The System Slot provides arbitration, clock distribution, and reset functions for all boards on the segment. The System Slot is responsible for performing system initialization by managing each local board's IDSEL signal. Physically, the System Slot may be located at any position in the backplane and **shall** be located on either end of the CompactPCI bus segment. For simplicity, this specification assumes one CompactPCI bus segment in which the System Slot is located on the left of the bus segment when the backplane is viewed from the front side.

The Peripheral Slots may contain simple boards, intelligent slaves, or PCI bus masters. Figure 2 illustrates the front view of a typical 3U CompactPCI segment.

Other topologies besides the linear arrangement illustrated in Figure 2 are allowed by CompactPCI. However, this specification and all backplane simulations have assumed a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing with the System Slot located on either end of the bus segment. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

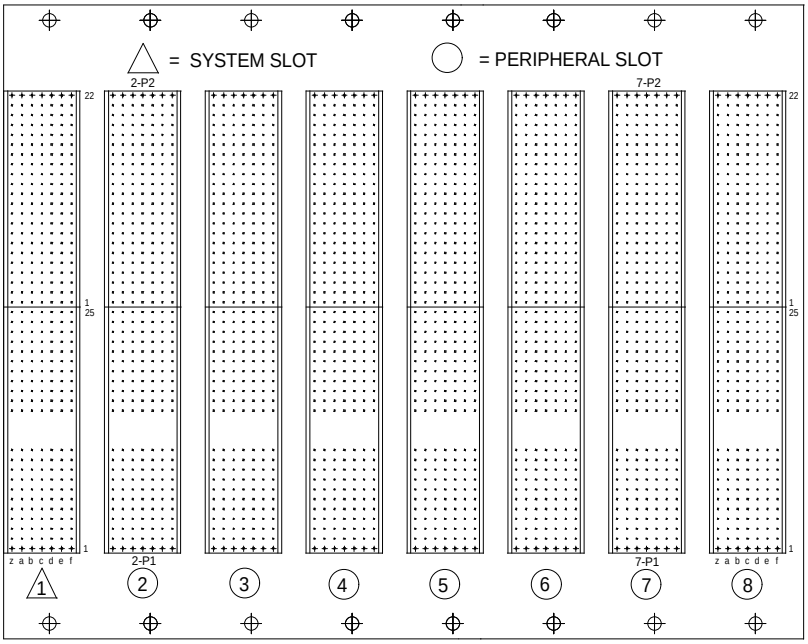


Figure 2. 3U CompactPCI Backplane Example.

CompactPCI defines slot numbering based on the concept of physical and logical slots. Physical slot numbers **shall** start at 1 in the top-left corner of the card cage. All CompactPCI systems **should** label all physical slots within the compatibility glyphs. Figure 2 illustrates an example of physical slot numbering within the compatibility glyphs (e.g., △1).

Logical slot numbers **shall** be defined by the IDSEL signal and associated address used to select the slot. Logical numbers are used in the nomenclature to define the physical outline of a connector on a bus segment. Logical numbers are illustrated in Figure 2 just below the connector outline (e.g., 2-P1). Logical and physical slot numbers **may** not always coincide. In either case, Chapter 3 defines signal routing requirements.

Capability glyphs provide visual indication of backplane connector and board capability. Capability glyphs are:

- △ (triangle) for System Slot
- ○ (circle) for Peripheral Slots

2.2 Connector

The CompactPCI connector is a shielded, 2 mm-pitch, 5-row connector as defined by IEC 917 and IEC 1076-4-101. Features of this connector include:

- Pin and socket interconnect mechanism
- Multi-vendor support
- Coding Mechanism providing positive keying
- Staggered make-break pin populations for optional hot swap capability
- Rear panel option for through-the-backplane I/O applications
- High density PCI capability
- Shield for EMI/RFI protection
- Expandability for end user applications

CompactPCI bus interconnection is defined as a 5 row by 47 position array of pins divided logically into two groups corresponding to the physical connector implementation. 32-bit PCI and connector keying are implemented on one connector (J1). An additional connector (J2) is defined for 64-bit transfers, for rear-panel I/O or for geographic addressing. See Section 5 for connector pin assignments and signal grouping.

The CompactPCI connector utilizes guide lugs located on the board connector to ensure correct polarized mating. Proper mating is further enhanced by the use of coding keys for 3.3 V or 5 V operation, with or without hot swap capability, to prevent incorrect installation of boards.

Coding keys prevent inadvertent installation of a 5 V board in a 3.3 V system. Table 1 illustrates the color coding that relates to different physical keys for the backplane connector and board connectors. Universal boards **shall** operate in either environment and are not keyed. Backplane connectors **shall** always be keyed according to the signaling level on the backplane segment.

Table 1. Coding Key Color Assignments.

Signaling Voltage V(I/O)	Color Reference
3.3 V	Cadmium Yellow
5 V	Brilliant Blue
3.3 V or 5 V (Universal Board)	None

2.3 Modularity

A key feature of CompactPCI is system modularity. Modularity is achieved by utilizing various Eurocard form factors along with a versatile 2 mm hard metric connector. Either the 3U or 6U form factor, or a combination of the two, **may** be used di-

rectly to create a system. The 2 mm HM connector is available in a variety of mechanical form factors for different applications.

2.4 Hot Swap Capability

The CompactPCI Connector provides three levels of pin staging within the backplane connector was originally defined to enable the implementation of hot swap. This pin staging was mandatory in previous revisions of this specification, and its use is an existing practice at the time of adoption of this specification. The PICMG Hot Swap Subcommittee no longer considers this pin staging viable. Other alternatives are under consideration for inclusion in a future “CompactPCI Hot Swap Specification.” See Section 5 for details on pin staging.

3. Electrical Requirements

This section documents the electrical requirements for CompactPCI boards and backplanes. CompactPCI boards plug into a backplane.

3.1 Board Design Rules

CompactPCI board design **shall** adhere to the design requirements for standard desktop PCI boards as specified in the PCI Specification. This section documents additional requirements and/or restrictions as needed. The design rules apply to PCI bus operation up to 33 MHz.

3.1.1 Decoupling Requirements

Each CompactPCI board **shall** have adequate decoupling. Table 2 illustrates the minimum requirements that **should** be used.

Table 2. Board Decoupling Requirements.

Connector	Mnemonic	Description	Decoupling Capacitance		Voltage(5)
			.1 µF ±20%(1)	10 µF ±20%(2)	
P1	5V	+5 VDC	✓	✓	15 V min.
P1	3.3V	+3.3 VDC	✓	✓	10 V min.
P1	V(I/O)	+5/3.3 VDC	✓	✓	15 V min.
P1	+12V	+12 VDC	✓	✓(3)	36 V min.
P1	-12V	-12 VDC	✓	✓(3)	36 V min.
P2(4)	V(I/O)	+5/3.3 VDC	✓	✓	15 V min.

Notes:

(1) For all voltages, one .1 µF ceramic capacitor suitable for high speed decoupling **shall** be provided close to the connector to decouple every 10 power pins. Note, this rule applies to all power pins even if unused on board.

(2) One 10 µf tantalum capacitor per voltage **shall** be located close to the connector (see note 3).

(3) Only required if ±12 V is used on board. Note, one .1 µF capacitor **shall** be provided on +12 V and –12 V even if unused on board.

(4) Requirements for P2 in a 64-bit system. If P2 is used for user defined I/O, additional decoupling capacitance may be required.

(5) Voltage values are three times the decoupled voltage value to avoid stressing a tantalum capacitor due to very fast power supply turn on times.

3.1.2 CompactPCI Signal Additions

CompactPCI defines some additional signals beyond the PCI specification that may be applicable to board designs. These signals are: Push Button Reset (PRST#), Power Supply Status (DEG#, FAL#), System Slot Identification (SYSEN#), System Enumeration (ENUM#), Geographic Addressing (GA[4..0]]), and legacy IDE interrupt support. Please refer to Section 3.2.8 for further descriptions.

3.1.3 Signal Termination

Many bussed PCI signals **shall** include a 10 Ω stub termination resistor located on the board at the CompactPCI connector interface. The signals that **shall** be terminated are: AD0-AD31, C/BE0#-C/BE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, DEVSEL#, PERR#, SERR#, and RST#.

Table 3. Stub Termination Resistor.

Parameter	Min.	Nominal	Max.	Units	Comment
R_{term}	-5%	10	+5%	ohms	Stub terminating resistor located at connector on board

If used by a board, the following signals **shall** also be terminated: INTA#, INTB#, INTC#, INTD#, SB0# , SDONE, AD32-AD63, C/BE4#-C/BE7#, REQ64#, ACK64#, and PAR64.

The following signals do not require a stub termination resistor: CLK, REQ#, GNT#, TDI, TDO, TCK, TMS, and TRST#.

The stub termination minimizes the effect of the stub on each board to the PCI backplane. The resistor **shall** be placed within 15.2 mm (0.6 inches) of the signal's connector pin. This length **shall** be included in the overall length of trace that is allowed for the signal as described in Sections 3.1.4 and 3.1.6.

Peripheral boards that drive REQ# **should** provide a series terminating resistor at the driver pin (not a stub termination resistor at the connector). On System Slot boards, a series resistor (sized according to the output characteristics of the clock buffer) **shall** be located at the driver for the CLK signal provided to each slot. Each System Slot board's GNT# signal **shall** also be series terminated at the driver with a resistor as required by the driving buffer output characteristics.

3.1.4 Peripheral Board Signal Stub Length

Signal length for 32-bit or 64-bit signals (J1) **shall** be less than or equal to 38.1 mm (1.5 inches). This length is measured from the connector pin through the stub or series termination resistor (described in Section 3.1.3) to the PCI device

pin. These lengths are consistent with the PCI Specification requirements but also include the resistor in the total trace length.

A maximum of one PCI load **shall** be allowed on any PCI signal from the connector on any given board. Peripheral boards with more than one load are not compliant with the CompactPCI Specification and **shall** not be declared CompactPCI compatible.

3.1.5 Characteristic Impedance

Boards **shall** be constructed within the characteristic impedance range given in Table 4.

Table 4. Board Characteristics.

Parameter	Min.	Nominal	Max.	Units	Comment
Z_0	-10%	65	+10%	ohms	PCB traces only

3.1.6 System Slot Board Loading

The System Slot **shall** have signal lengths less than or equal to 63.5 mm (2.5 inches) for 32-bit or 64-bit boards.

The System Slot **may** have two PCI loads on each signal on a PCI backplane segment to accommodate practical implementations of PCI-based CPU designs. If an additional load is added on the System Slot board, only one stub termination resistor per PCI signal **shall** be required as defined in Section 3.1.3.

3.1.7 Peripheral Board PCI Clock Signal Length

On Peripheral boards, the PCI clock signal length **shall** be 63.5 mm ± 2.54 mm (2.5 inches ±0.1 inches), and **shall** drive only one load on the board.

3.1.8 Pull-Up Location

Pull-up resistors required by the PCI specification **shall** be located on the System Slot board. Table 5 provides minimum, typical, and maximum values for both 5 V and 3.3 V signaling environments. All values assume nine loads (two on the System Slot board plus one each on seven other boards) and ± 10% resistor values. The pull-up resistor, for those signals requiring a pull-up, **shall** be placed on the in-board side of the stub termination resistor.

Table 5. Pull-up Resistor Values.

Signaling Voltage	R_{min}	$R_{typical}$	R_{max}
5 V	1.0 KΩ	2.0 KΩ	3.0 K
3.3 V	2.7 KΩ	5.1 KΩ	8.2 KΩ

The System Slot board **shall** provide a pull-up resistor for the REQ64# and ACK64# signals even if the System Slot board does not use these signals, as in the case of a 32-bit System Slot board. This requirement accommodates 64-bit boards. They **shall** see the signal REQ64# as false during reset to properly connect to the 32-bit PCI bus. The pull-up resistor also prevents floating REQ64# or ACK64# signals on 64-bit boards.

The only pull-up resistor CompactPCI requires beyond the PCI specification is located on each bus master utilizing the GNT# signal. Each board using GNT# **shall** have a 100 KΩ pull-up resistor to prevent a floating input if GNT# is not being driven by the System Slot board.

3.1.9 Connector Shield Requirements

The CompactPCI connector **shall** load a shield at row F on the board. This shield covers the top of the IEC-1076 connector and helps to provide a low impedance return path for ground between the board and the CompactPCI backplane. Boards that do not use this shield are not compliant and are not guaranteed to work in all CompactPCI system topologies.

The lower shield option that is provided for in the IEC-1076 connector is not required for CompactPCI boards and **shall** not be loaded if it protrudes into the interboard separation plane.

3.1.10 Front Panel I/O Connector Recommendations

CompactPCI boards **should** utilize metalized shell connectors for EMI/RFI protection. The shell **should** be electrically connected to the I/O plate through a low impedance path in accordance with IEEE 1101.10.

The I/O plate is assumed to be connected to earth ground and isolated from logic ground. CompactPCI boards **shall** not connect earth ground (on front panel) through a low impedance path to logic ground used on board.

3.2 Backplane Design Rules

CompactPCI defines a backplane environment that **may** have up to eight slots. One slot, the System Slot, provides the clocking, arbitration, configuration, and interrupt processing for the other seven slots. Fewer slots may be provided in a CompactPCI backplane, but the following sections assume that a maximum configuration is employed in a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing with the System Slot located on either end of the bus segment. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

Backplanes **shall** provide separate power planes for 3.3 V, 5 V, and ground. If V(I/O) is configurable as 3.3 V or 5 V, then a separate power plane **shall** be dedicated for V(I/O).

3.2.1 Characteristic Impedance

Boards **shall** be constructed within the characteristic impedance range given in Table 6.

Table 6. Backplane Characteristics.

Parameter	Min.	Nominal	Max.	Units	Comment
Z_0	-10%	65	+10%	ohms	PCB without connectors or boards installed

3.2.2 Eight-Slot Backplane Termination

System simulation has shown that when using the strongest PCI buffer allowed (refer to the PCI specification V-I curves) and with a lightly loaded eight-slot backplane configuration with the System Slot and logical Slot 2 loaded (only two boards), that the 10 ns maximum propagation delay for PCI signals is violated. To address this, fast Schottky diode signal termination (Reference Texas Instruments 74S1053 diode array) **shall** be added to the end of the backplane furthest from the System Slot, as illustrated in Figure 3. The diodes **shall** be added directly to the backplane or via a Peripheral board in the slot furthest away from the System Slot.

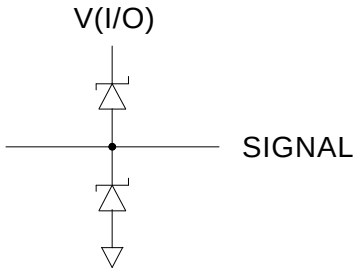


Figure 3. PCI Signal Termination.

3.2.3 Clock Routing Requirements

A 2 ns maximum skew **shall** be maintained between any two PCI components (not connector to connector) per PCI specification requirements. Adherence to backplane and board rules contained in this specification help meet this requirement.

The System Slot board drives five buffered clocks via CLK0-CLK4 (pins J1:D6, J2:A1, J2:A2, J2:B2, and J2:A3) and **should** drive two additional buffered clocks via CLK5-CLK6 (pins J2:A20 and J2:A21). On backplanes, board slots receive their specific clock using the CLK pin (J1:D6). Table 7 illustrates the CLK0-CLK4 to board slot connections. Note backplane clock routing at the time of adoption of this specification only support clocks CLK0-CLK4. CLK5-CLK6 provided by the System Slot board to support a future hot swap specification are not routed on the backplane.

To minimize signal reflections, the clock connection for Peripherals in logical Slots 2/3 and 4/5 **shall** be physically connected in the manner illustrated in Figure 4. Board slots 6-8 have a direct connection from the System Slot as illustrated in Figure 5.

For seven-slot backplanes, only logical slots 2 and 3 need to share CLK0. For backplanes with six or fewer slots, each slot **shall** have a dedicated clock.

See Section 3.3 for further details.

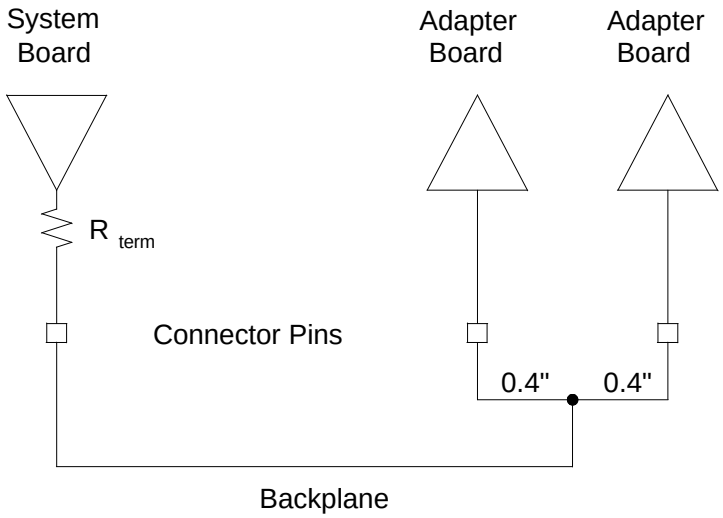


Figure 4. Physical Clock Routing Requirements for Logical Slots 2/3 and 4/5.

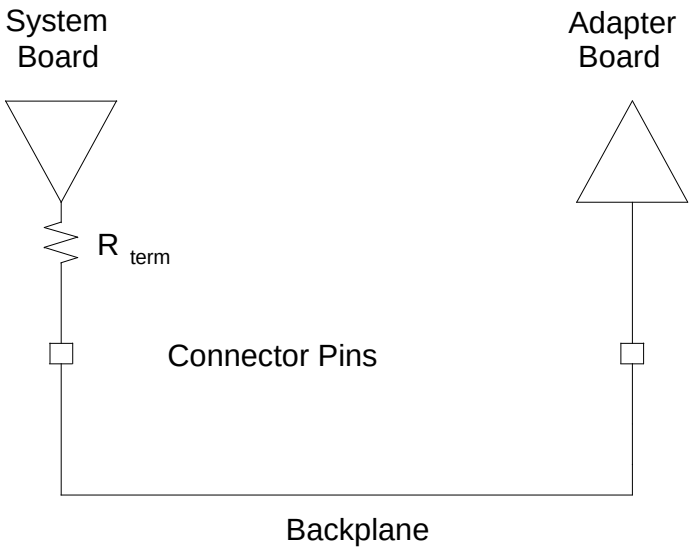


Figure 5. Physical Clock Routing Requirements for Logical Slots 6-8.

3.2.4 Signaling Environment

Each CompactPCI backplane provides for either a 5 V or 3.3 V signaling environment. PCI allows for two types of buffer interfaces for interboard connection. 5 V signaling will generally be used for early systems. A gradual shift to 3.3 V will occur as the semiconductor industry shifts to the lower power interface for speed and power dissipation reasons. The V(I/O) power pins on the connector are used to power the buffers on the peripheral boards, allowing a card to be designed to work in either interface.

CompactPCI allows for this dual interface scheme by providing a unique backplane connector coding plug for either system. The CompactPCI backplane may be either a fixed signaling environment backplane (e.g., 5 V only) or may be configurable. In any case, when configured for 5 V operation, the 5 V coding plug (Brilliant Blue) **shall** be used, and when configured for 3.3 V operation, the 3.3 V coding plug (Cadmium Yellow) **shall** be installed in the backplane connector.

With the above mechanism, boards that have the coding plug matching the backplane can be inserted. The opposite technology board is likewise inhibited from being inserted. Boards that are either 3.3 V or 5 V **shall** not have a coding plug and therefore can be inserted in either system. Refer to Sections 5.5 and 5.6 for details.

3.2.5 IDSEL Assignment

The PCI signal IDSEL is used to provide unique access to each logical slot for configuration purposes. By connecting one of the address lines AD31 through AD25 to each board's IDSEL pin (J1:B9), a unique address for each board is provided during configuration cycles. Table 7 illustrates the assignment of ad-

dress lines to each board's IDSEL pin. The backplane **shall** make the connection to IDSEL at each logical slot's connector with minimum trace length.

One additional PCI device on the CompactPCI bus segment is allowed on the System Slot board. This device and additional PCI devices on a System Slot CPU board (i.e., a bridge is being used) **may** be selected using lower ADxx lines in the range of AD11 to AD24.

3.2.6 REQ#/GNT# Assignment

The System Slot interfaces to seven pairs of REQx#/GNTx# pins called REQ0#-REQ6# and GNT0#-GNT6#. Each board slot interfaces to one pair of REQx#/GNTx# signals using pins called REQ# (J1:A6) and GNT# (J1:E5). Table 7 lists the assignment of request/grant signals to each board's REQ# and GNT# pins.

The System Slot on any given CompactPCI backplane segment **shall** support the full complement of REQ#/GNT# signals.

The System Slot board **should** support seven pairs of REQx#/GNTx# signals for a system in which there are seven peripheral PCI bus masters.

If a System Slot board cannot support the full complement of REQ#/GNT# signals, provision **shall** be made to configure which slots in the CompactPCI backplane are supported for arbitration. In this manner, boards using REQ#/GNT# signals may be located in any given slot as required by the application.

Observation: The System Slot board uses the pins labeled REQ# and GNT# as REQ0# and GNT0#, respectively. CLK1 and CLK0 are correct in Table 4, although they seem reversed. This was done to facilitate trace routing and maintain equal trace lengths to minimize skew.

Table 7. System to Logical Slot Signal Assignments.

Signal	Connector:Pin	Signal	Connector:Pin
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 2**	
CLK1[1]	P2:A1	CLK	P1:D6
AD31	P1:E6	IDSEL[3]	P1:B9
REQ0#	P1:A6	REQ#	P1:A6
GNT0#	P1:E5	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 3**	
CLK1[1]	P2:A1	CLK	P1:D6
AD30	P1:A7	IDSEL[3]	P1:B9
REQ1#	P2:C1	REQ#	P1:A6
GNT1#	P2:D1	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 4**	
CLK0[1]	P1:D6	CLK	P1:D6
AD29	P1:B7	IDSEL[3]	P1:B9
REQ2#	P2:E1	REQ#	P1:A6
GNT2#	P2:D2	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 5**	
CLK0[1]	P1:D6	CLK	P1:D6
AD28	P1:C7	IDSEL[3]	P1:B9
REQ3#	P2:E2	REQ#	P1:A6
GNT3#	P2:C3	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 6**	
CLK2	P2:A2	CLK	P1:D6
AD27	P1:E7	IDSEL[3]	P1:B9
REQ4#	P2:D3	REQ#	P1:A6
GNT4#	P2:E3	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 7**	
CLK3	P2:B2	CLK	P1:D6
AD26	P1:A8	IDSEL[3]	P1:B9
REQ5#[2]	P2:D15	REQ#	P1:A6
GNT5#[2]	P2:E15	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 8**	
CLK4	P2:A3	CLK	P1:D6
AD25	P1:D8	IDSEL[3]	P1:B9
REQ6#[2]	P2:D17	REQ#	P1:A6
GNT6#[2]	P2:E17	GNT#	P1:E5

Notes:

(1) CLK0 and CLK1 are reversed to facilitate trace routing and maintain equal trace lengths to minimize skew.

(2) System Slot boards that do not support seven REQ#/GNT# signals **shall** provide a mechanism to connect any Peripherals in logical slots 2-8 that may need arbitration service depending on the board installed.

(3) The IDSEL signal at each slot **shall** be connected with minimal trace length at the slot that is intended. For example, at logical slot 6, IDSEL **shall** be connected to AD27 with minimal trace length.

3.2.7 PCI Interrupt Binding

Interrupt binding of the BIOS setup program **shall** require backplane assignments from the System Slot interrupt pins INTA#-INTD# to the logical board slot interrupts as defined in Table 8.

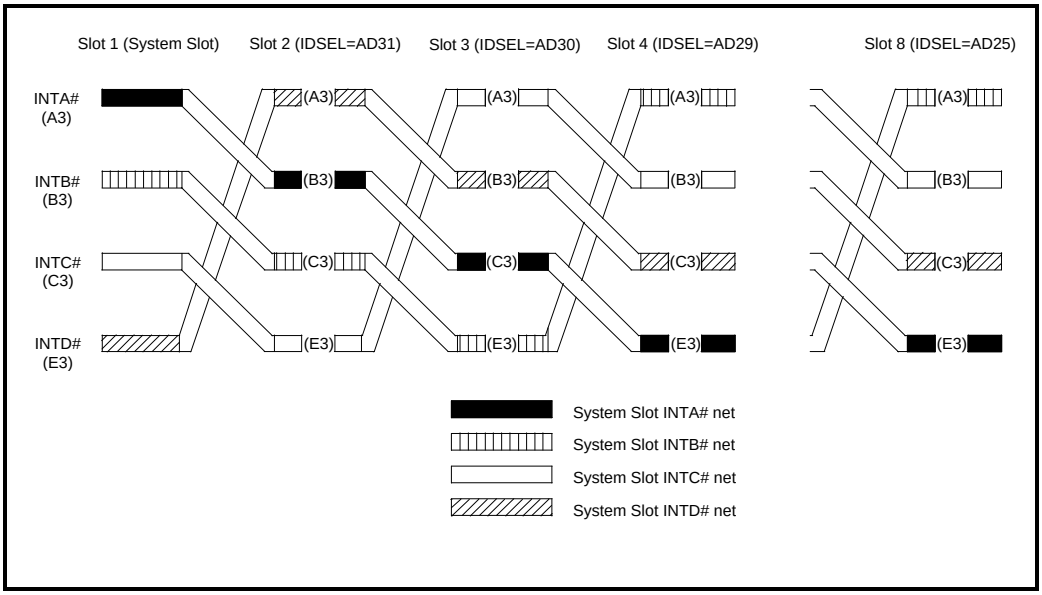
Backplane assignments rotate through logical board slots to provide a unique PCI interrupt to each board for the first four PCI connectors (assuming that each board drives just its INTA# signal). Rotating interrupt assignments allows multiple PCI peripherals that drive only INTA# in order to utilize a different interrupt on the System Slot board without the need to share an interrupt with another PCI interface. Since multi-function PCI devices are allowed to drive more than one interrupt, shared interrupts may be required even within the first four board slots. In addition, the rotating pattern repeats itself after logical slot four, which also requires the sharing of an interrupt for slots that are four connectors apart (logical slots 2 and 6 for example).

The Interrupt assignments are consistent with the PCI-PCI Bridge Specification as defined by the PCI SIG. This is to allow PCI-PCI bridge technology on CPU boards between Bus 0 and CompactPCI.

Although PCI software device drivers are designed to allow sharing of interrupt signals, sharing an interrupt with another device can affect interrupt latency and is generally avoided where possible.

Please see Section 3.2.8.4 for interrupt support for legacy IDE devices.

Table 8. System to Logical Slot Interrupt Assignments.



3.2.8 CompactPCI Signal Additions

CompactPCI utilizes PCI signals as defined by the *PCI Local Bus Specification* with some additional signals. These additional signals do not affect the PCI sig-

nals but **may** enhance system operation by providing push button reset, power supply status, System Slot identification, geographic addressing, and legacy IDE interrupt support features.

3.2.8.1 Push Button Reset (PRST#)

PRST# **may** be used in a CompactPCI system to reset the System Slot board, which in turn would reset the rest of the system using the PCI RST# signal. PRST# is an active low true TTL signal generated by a switch closure or an open-collector driver. It is the responsibility of the System Slot board receiving PRST# to debounce it as required. The System Slot board **shall** terminate PRST# with a pullup resistor as defined in Section 3.1.8.

3.2.8.2 Power Supply Status (DEG#, FAL#)

Power supply status **may** be determined from two low true TTL power supply status signals available on backplanes utilizing modular power supplies implementing the optional DEG# and FAL# signals. The System Slot board **shall** terminate both signals with a pullup resistor as defined in Section 3.1.8, even if the system board does not use these signals. Please see Section 3.2.9.2 for more information.

3.2.8.3 System Slot Identification (SYSEN#)

This pin is grounded on the CompactPCI backplane segment at the System Slot so the board **may** identify installation into the System Slot. This pin is not connected on the backplane for the remaining slots. Boards that sense this signal **shall** provide their own pull-up to V(I/O) and disable all System Slot functions, such as clock generation and bus arbitration when it is not installed in a System Slot.

3.2.8.4 Legacy IDE Interrupt Support

Two additional non-PCI interrupts are defined for IDE boards. Both primary and secondary ISA interrupts, designated INTP and INTS respectively, are available and **may** be used by the master. The System Master **should** route the INTP (pin D4) and INTS (pin E4) on board to interrupt requests IR14 and IR15, respectively. These signals are active high TTL level signals and do not have the requirement of meeting the PCI electrical buffer characteristics. INTP and INTS are provided to ease the transition from Compatibility Mode to Native Mode PCI IDE operation.

Compatibility Mode forces the IDE controller to be I/O mapped at the PC-AT location (1F0h-1F7h and 3F6h-3F7h), as well as forcing the use of IR14 and IR15 for hard disk interrupts.

Native Mode operation allows the IDE controller to be mapped at any location and also allows any unused interrupt to be used for the interface.

3.2.8.5 System Enumeration (ENUM#)

This low true TTL open-collector signal **shall** be driven by hot swap compatible boards after insertion and prior to removal. The System Master uses this interrupt signal to force software to interrogate all boards within the

system for resource allocation regarding I/O, memory, and interrupt usage. The System Slot board **shall** terminate ENUM# with a pullup resistor as defined in Section 3.1.8. Newly inserted boards will have resources allocated to them (if available). Boards that are about to be removed will be providing early status to the operating system and/or application that it will soon be unavailable. Consult the CompactPCI Hot swap Specification for further details.

3.2.8.6 Geographic Addressing (GA[4..0])

For backplanes that implement the 64-bit connector pin assignments, the signals GA[4..0] on the top five pins of the J2/P2 connector, **shall** be available for use by 64-bit boards and **may** be used by 32-bit boards to provide a unique differentiation based upon which physical slot the board has been inserted. Backplanes that implement the Rear-Panel I/O connector pin assignments for J2/P2 **may** support geographic addressing.

Boards that support the JTAG multi-drop can use these signals to provide a unique address within the system. Each signal **shall** be pulled up with a 10.0 KΩ ±10% resistor on any board using the geographic addressing signals GA[4..0].

For backplanes that implement the 64-bit connector pin assignments, the physical slot address (GA[4..0]) **shall** be encoded on the backplane by grounding and leaving unconnected different combinations of pins at each connector. Physical slot addresses are defined by the physical slot number per Section 2.1. Table 9 illustrates the physical slot number and its physical slot address defined by GA[4..0]. Physical slot numbers “0” and “31” are reserved for future use.

Table 9. Physical Slot Addresses.

Physical Slot Number	GA[4] (J2-A22)	GA[3] (J2-B22)	GA[2] (J2-C22)	GA[1] (J2-D22)	GA[0] (J2-E22)
0(1)	GND	GND	GND	GND	GND
1	GND	GND	GND	GND	Open
2	GND	GND	GND	Open	GND
3	GND	GND	GND	Open	Open
4	GND	GND	Open	GND	GND
5	GND	GND	Open	GND	Open
6	GND	GND	Open	Open	GND
7	GND	GND	Open	Open	Open
8	GND	Open	GND	GND	GND
9	GND	Open	GND	GND	Open
10	GND	Open	GND	Open	GND
11	GND	Open	GND	Open	Open
12	GND	Open	Open	GND	GND
13	GND	Open	Open	GND	Open
14	GND	Open	Open	Open	GND
15	GND	Open	Open	Open	Open
16	Open	GND	GND	GND	GND
17	Open	GND	GND	GND	Open
18	Open	GND	GND	Open	GND
19	Open	GND	GND	Open	Open
20	Open	GND	Open	GND	GND
21	Open	GND	Open	GND	Open
22	Open	GND	Open	Open	GND
23	Open	GND	Open	Open	Open
24	Open	Open	GND	GND	GND
25	Open	Open	GND	GND	Open
26	Open	Open	GND	Open	GND
27	Open	Open	GND	Open	Open
28	Open	Open	Open	GND	GND
29	Open	Open	Open	GND	Open
30	Open	Open	Open	Open	GND
31(1)	Open	Open	Open	Open	Open

Note:

(1) Physical slot numbers “0” and “31” are reserved for future use.

3.2.9 Power Distribution

Power is distributed in a CompactPCI system by utilizing a backplane. Each backplane **shall** make provisions for the standard regulated direct current (DC) supply voltages in Table 10 below.

Table 10. Power Specifications.

Mnemonic	Description	Nominal Value	Tolerance	Max. Ripple
5 V	+5 VDC	5.0 V	±5%	50 mV(1)
3.3 V	+3.3 VDC	3.3 V	±5%	50 mV(1)
+12 V	+12 VDC	12.0 V	±5%	50 mV(1)
-12 V	-12 VDC	-12.0 V	±5%	50 mV(1)
GND	Ground			

Note:

(1) Maximum ripple is very difficult to accurately measure and therefore requires good measurement techniques. Measurement should be made at full load at 20 MHz bandwidth with a 22 µF and .1 µF capacitor located at the measurement point.

The backplane **shall** provide power connectors for all of the supply voltages in Table 10. One of two methods **may** be chosen:

- Power terminals **may** be located on the front or rear side of the backplane for external power sources.
- An IEC 603-2 (DIN 41612) style connector and rear side power terminals **should** be used for in-rack modular power supplies.

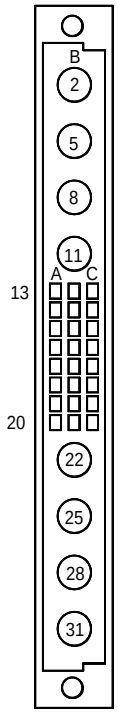
3.2.9.1 External Power Connections

Several styles of high current printed circuit board terminals are available. At least one per supply voltage **shall** be provided.

3.2.9.2 In-Rack Power Connections

Connectors compliant with IEC 1076 or IEC 603-2, with high current pins, **may** be used to input AC or DC power to the supply and output the regulated DC voltages. An IEC 603-2 connector and pin assignment suitable for providing 30 A at 5 VDC with remote sensing and 12 A at 3.3 VDC without remote sensing is illustrated in Figure 6. This connector is specified because its use was mandatory for in-rack modular power supplies in a previous revision of this specification, and its use is an existing practice at the time of adoption of this specification. Other connectors **may** be used when the connector and pin assignment specified here do not meet system requirements.

The female connector is located on the backplane and the male is located on the power supply.



Pin #[1]	Staging[2]	Mnemonic	Description
Column A			
A13	EL	SP	Spare
A14	EL	INH#	Inhibit Signal
A15	EL	ISH	Current Share Signal
A16	EL	5S-	5 V Sense -
A17	EL	5S+	5 V Sense +
A18	EL	3.3V	+3.3 VDC
A19	EL	+12V	+12 VDC
A20	EL	-12V	-12 VDC
Column B			
B2	SL	ACL	AC Line
B5	SL	ACN	AC Neutral
B8	-	-	No Pin Loaded
B11	EL	CG	Chassis Ground
B13	SL	3.3V	+3.3 VDC
B14	SL	3.3V	+3.3 VDC
B15	SL	3.3V	+3.3 VDC
B16	SL	3.3V	+3.3 VDC
B17	SL	3.3V	+3.3 VDC
B18	SL	3.3V	+3.3 VDC
B19	SL	+12V	+12 VDC
B20	SL	-12V	-12 VDC
B22	EL	5V	+5 VDC
B25	EL	GND	Ground
B28	EL	+DC	+DC Input
B31	EL	-DC	- DC Input
Column C			
C13	SL	EN#	Enable Signal
C14	SL	DEG#	Derate Signal
C15	SL	FAL#	Supply Fail Signal
C16	SL	3.3V	+3.3 VDC
C17	SL	3.3V	+3.3 VDC
C18	SL	3.3V	+3.3 VDC
C19	SL	+12V	+12 VDC
C20	SL	-12V	-12 VDC

Notes:

1. Pin numbers illustrated are of the female backplane connector.
2. EL is an Extra Length pin. SL is a Standard length pin.

Figure 6. Modular Power Supply Connector.

Backplanes providing an in-rack modular power connector **shall** provide connections for the optional DEG# and FAL# interrupt signals described below.

A brief description of the modular power connector signals illustrated in Figure 6 follows:

INH# *Inhibit* signal **may** be used to “turn off” the power supply outputs. This signal is on a longer pin than the EN# (enable) signal and therefore has precedence over the EN# signal when determining power supply operation (see Table 11). The INH# signal is typically connected to an “ON/OFF” switch. This signal is optional.

Table 11. Modular Power Supply Operation.

INH# =	Low	Low	High	High
EN# =	Low	High	Low	High
Power Status	“OFF”	“OFF”	“ON”	“OFF”

ISH *Current Share* signal **may** be used between multiple power supplies for load balancing. This signal is not required for single power supply systems.

Observation: Because implementation and timing for ISH may vary from manufacturer to manufacturer, interoperability between two or more power supplies from different manufacturers is not guaranteed.

5S- *5 V Sense* - **shall** be connected to the center of the ground plane for accommodating power distribution losses. This signal is required for all modular power supplies.

5S+ *5 V Sense* + **shall** be connected to the center of the power plane for accommodating power distribution losses. This signal is required for all modular power supplies.

ACL *AC Line* input **shall** be used for supplies operating from AC. This input is not required for DC input power supplies. Separate AC and DC inputs are provided to prevent damaging an AC power supply inserted into a backplane wired for DC and visa versa.

ACN *AC Neutral* input **shall** be used for supplies operating from AC. This input is not required for DC input power supplies.

+DC *Positive DC* input **shall** be used for supplies operating from DC. This input is not required for AC input power supplies. Separate AC and DC inputs are provided to prevent damaging a DC power supply inserted into a backplane wired for AC and visa versa.

-DC *Negative DC* input **shall** be used for supplies operating from DC. This input is not required for AC input power supplies.

EN# *Enable* signal **may** be used to “turn on” the power supply outputs. EN# is used in conjunction with INH# (see Table 11) and is typically connected to ground to enable the power supply after other signals on longer pins have made contact. This signal is optional.

DEG# *Derating* signal **may** be used as an output from the power supply to indicate that the supply is beginning to derate its power output. This signal is optional. Note that backplanes providing a modular power supply connector **shall** connect DEG# to the backplane signal DEG# (P2:C16) in the event that a power supply implementing this signal is installed.

FAL# *Supply Fail* signal **may** be used as an output from the power supply to indicate that it has failed. This signal is optional. Note that back-

planes providing a modular power supply connector **shall** connect FAL# to the backplane signal FAL# (P2:C15) in the event that a power supply implementing this signal is installed.

All other signals given in Figure 6 are required and **shall** be provided by the modular power supply.

3.2.10 Power Decoupling

CompactPCI boards may utilize any of the voltages in Table 10. Without adequate power decoupling on the backplane for the 5 V and 3.3 V power, intermittent operation may result. The backplane has dedicated 5 V and 3.3 V power pins along with V(I/O) power pins. The V(I/O) power pins are connected to either 5 V or 3.3 V depending on if 5 V or 3.3 V backplane signals are being used. See Section 5.5.

All power voltages **shall** be decoupled to ground in such a manner as to provide for reasonable management of switching currents (di/dt). Low impedance power planes and connections to low equivalent series resistance (ESR) capacitors should be used. Even if a system does not use 3.3 or 5 V, the unused power pins **shall** be connected and decoupled to provide an additional AC return path. Table 12 illustrates the bypass guidelines that **should** be used for each connector.

Table 12. Backplane Decoupling Recommendations.

Mnemonic	Description	Decoupling Capacitance	Voltage(2)
5V	+5 VDC	44 μF ± 20% (1)	15 V min.
3.3V	+3.3 VDC	44 μF ± 20% (1)	10 V min.
V(I/O)	+5/3.3 VDC	44 μF ± 20% (1)	15 V min.
+12V	+12 VDC	15 μF ± 20%	36 V min.
-12V	-12 VDC	15 μF ± 20%	36 V min.

Note:

(1) Recommended decoupling capacitance per connector best distributed across the length of each connector.

(2) Voltage values are three times the decoupled voltage value to avoid stressing a tantalum capacitor due to very fast power supply turn on times.

3.3 PCI Clock Distribution

The System Slot board **shall** provide clock signals for all PCI peripherals in the system, including devices on the System Slot board. Peripheral boards are provided clock signals via the CompactPCI backplane. A maximum skew of 2 ns **shall** be maintained across the system operating at 33 MHz between any two PCI devices at the clock input of the integrated circuits.

Clock skew is the difference between the maximum and minimum propagation delay of any PCI clock signal. There are two components that contribute to clock skew in a CompactPCI system:

1. Backplane Clock Skew. The CompactPCI backplane provides the distribution of clock signals for all of the board slots in the system. The differences in the trace routing and net topologies contribute to skew and also define the longest clock delay that **shall** be considered in the design of the system and still meet overall system clock skew requirements.
2. System Slot Board Clock Skew. This is the clock skew that **may** be attributed to the onboard routing differences (if any) of all of the PCI clocks as well as the skew specification for the type of integrated circuit driver used for clock distribution. The onboard clock routing **shall** be designed to complement the propagation delays of distributing the clock to a backplane and still meet overall system skew requirements.

3.3.1 Backplane Clock Routing Design Rules

CompactPCI backplanes **shall** be designed to provide a consistent environment for System Slot boards with regard to backplane clock routing. Design rules assume a linear backplane with the System Slot at one end of the bus segment and 20.32 mm (0.8 inch) connector spacing.

Note, backplane clock routing at the time of adoption of this specification only support clocks CLK0-CLK4. CLK5-CLK6 provided by a System Slot board are left unconnected on the backplane.

3.3.1.1 Backplanes that are Six-Slots or Fewer

For CompactPCI Backplanes that are six-slots or fewer (including the System Slot), each board slot **shall** be provided a discrete clock signal, with the routing on the backplane matched within 50 mm (2 inches) for all clock signals. Note that CLK and CLK1 may need to be routed with additional trace length to meet these requirements. No clock length may exceed 185 mm (7.3 inches) in length.

3.3.1.2 Backplanes that are Seven-Slots

These backplanes share a clock signal between logical slots 2 and 3. Logical board slots 4-7 all have discrete clock routing and **should** be routed within 50 mm (2 inches) of each other in length. No clock routed to logical slots 4-8 **shall** exceed 185 mm (7.3 inches) in length. The shared clock connected to logical slots 2 and 3 **shall** be shorter than or equal to 81.3 mm (3.2 inches).

3.3.1.3 Backplanes that are Eight-Slots

These backplanes share a clock signal between logical slots 2 and 3 and also logical slots 4 and 5. Logical board slots 6-8 all have discrete clock routing and **should** be routed within 50 mm (2 inches) of each other in length. No clock routed to logical slots 6-8 **shall** exceed 185 mm (7.3 inches) in length. The shared clock connected to logical slots 2 and 3 **shall** be shorter than or equal to 81.3 mm (3.2 inches). The shared clock connected to logical slots 4 and 5 **shall** be shorter than or equal to 76.2 mm (3 inches).

3.3.2 System Slot Board Clock Routing Design Rules

The System Slot clock distribution circuitry **shall** be designed to accommodate up to 1.2 ns of backplane skew (minimum vs. maximum number of slots and various loading configurations). The following design rules apply to clock distribution to backplane peripherals and local (onboard) PCI peripherals.

3.3.2.1 Clock Routing to Connector Clock Pins

The clock distribution circuitry on the System Slot **shall** provide a discrete clock signal to each of the CompactPCI connector pins defined as a PCI clock (CLK, CLK1, CLK2, CLK3, CLK4). Additionally, the System Slot board **should** drive two more buffered clocks via CLK5-CLK6 (pins J2:A20 and J2:A21) even though backplanes are not required to route the signals at the time this specification was adopted. By providing these two additional clocks, support for a future hot swap specification is provided. The routing of these signals **shall** be matched in length.

3.3.2.2 Clock Routing to Local PCI Peripherals

Any onboard PCI peripherals, including PCI to PCI bridges, **shall** be provided a clock that is delayed to accommodate the maximum propagation delay of the backplane clocks and still meet the 2 ns overall skew requirement. Up to 800 ps of skew is allowed for onboard clock distribution (including the clock buffer internal skew). The onboard clock signals **shall** be delayed beyond the clocks routed to the backplane (Section 3.3.2.1) to accommodate best and worst case backplane skews. Sample Spice models for the backplane clock nets are available from PICMG to assist CPU designers in determining the onboard delay for their design.

4. Mechanical Requirements

4.1 Board Requirements

CompactPCI connector pin numbering is intentionally different from the connector manufacturer's pin numbering. This was done to allow the connectors to start at the bottom of the board and "grow" upward from J1/P1 through J5/P5.

4.1.1 Physical Outlines

CompactPCI defines two board sizes, 3U and 6U.

4.1.1.1 3U Boards

3U boards are 100 mm by 160 mm. The PCB is 1.6 mm thick. A 2 mm (IEC-1076-4-101) connector is used for interfacing to the CompactPCI bus segment. Figure 7 illustrates the 3U board dimensions and connector location. 32-bit PCI is implemented on J1. J2 **may** be used for 64-bit PCI signaling, rear-panel I/O, or System Slot functions.

Note that row Z is not present on connectors J1 and J2 used on system or peripheral boards. Refer to IEC-1076-4-101 documentation for details.

4.1.1.2 6U Boards

6U boards are 233.35 mm by 160 mm. Figure 8 illustrates the 6U board dimensions and connector locations J1, J2, J3, J4 and J5. 32-bit PCI is implemented on J1. J2 is used for 64-bit PCI signaling, rear-panel I/O, or System Slot functions. J3, J4 and J5 **may** be used for rear-panel I/O.

Rear-panel I/O **may** be defined by the user and/or utilize PICMG specifications. Contact PICMG for copies of these specifications.

Note that row Z is not present on connectors J1 and J2 used on system or peripheral boards. Refer to IEC-1076-4-101 documentation for details.

4.1.1.3 Rear-panel I/O Boards

Rear-panel I/O boards may be either 3U (100 mm) or 6U (233.35 mm) in height and are typically 80 mm in depth. Figure 9 illustrates an 80 mm representative rear-panel I/O board defined by IEEE P1101.11. Other depths as defined by IEEE P1101.11 are allowed depending on the application requirements. Refer to IEEE P1101.11 for further details.

4.1.2 Cross Sectional View

Figure 10 provides a cross sectional view illustrating the relationship between the front panel, board, connectors, and backplane. Refer to IEEE 1101.1 and IEEE 1101.10 (EMC) for additional details. Note that the top connector shield (component side) **shall** be installed to meet the electrical requirements. The bottom connector shield (back side) **may** be installed if it does not protrude into the interboard separation plane.

4.1.3 Component Outline and Warpage

The sum of warpage and component lead lengths or components **shall** be less than or equal to 1.52 mm (0.060 inch) from where the solder side of an ideal (no warpage) board would be. The sum of component height and warpage **shall** be less than or equal to 13.71 mm (0.540 inch) from the component side of an ideal (no warpage) board. Refer to IEEE 1101.1 for additional information. Figure 11 illustrates the connector, lead length, and component outlines.

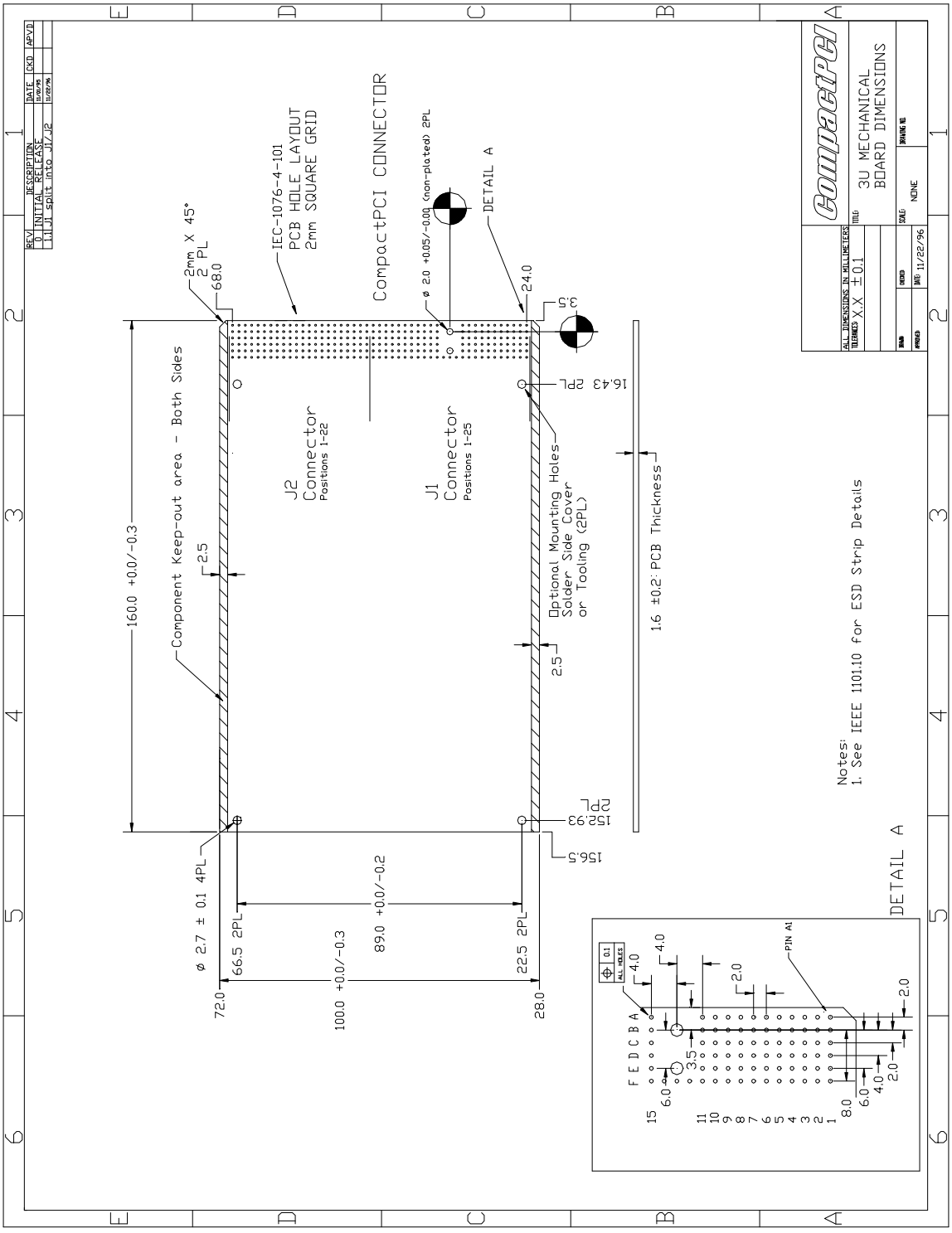


Figure 7. 3U Board.

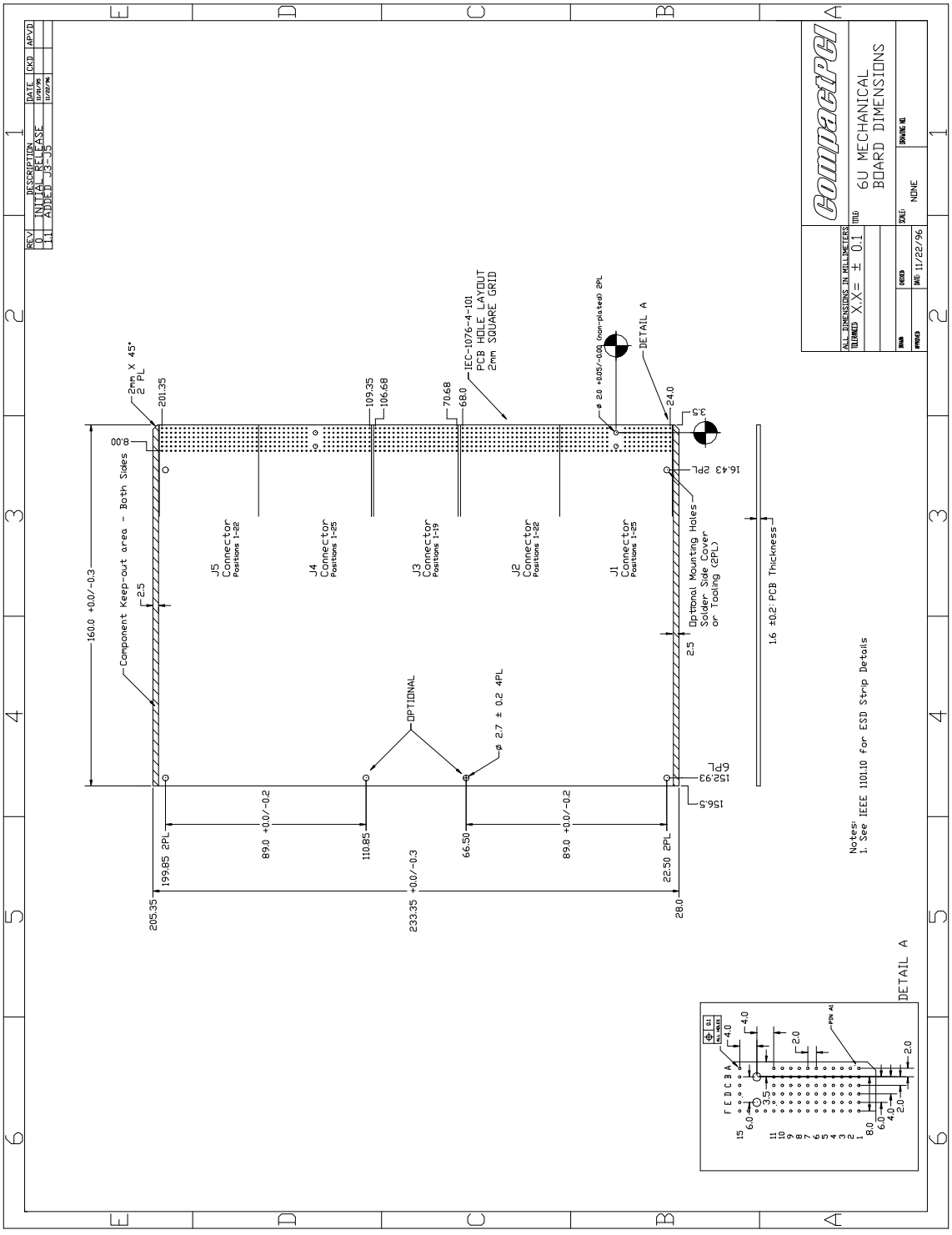


Figure 8. 6U Board.

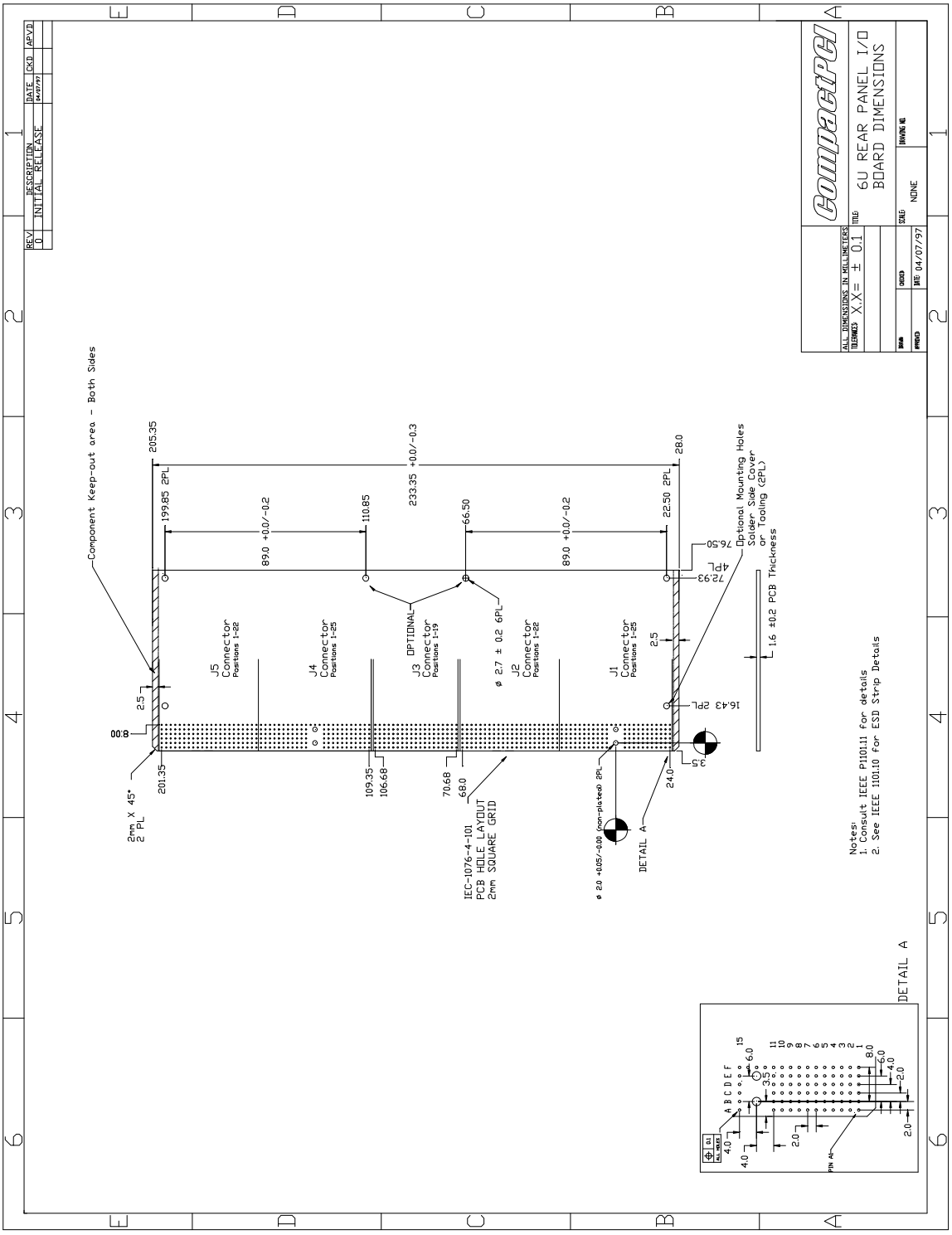


Figure 9. Rear-Panel I/O

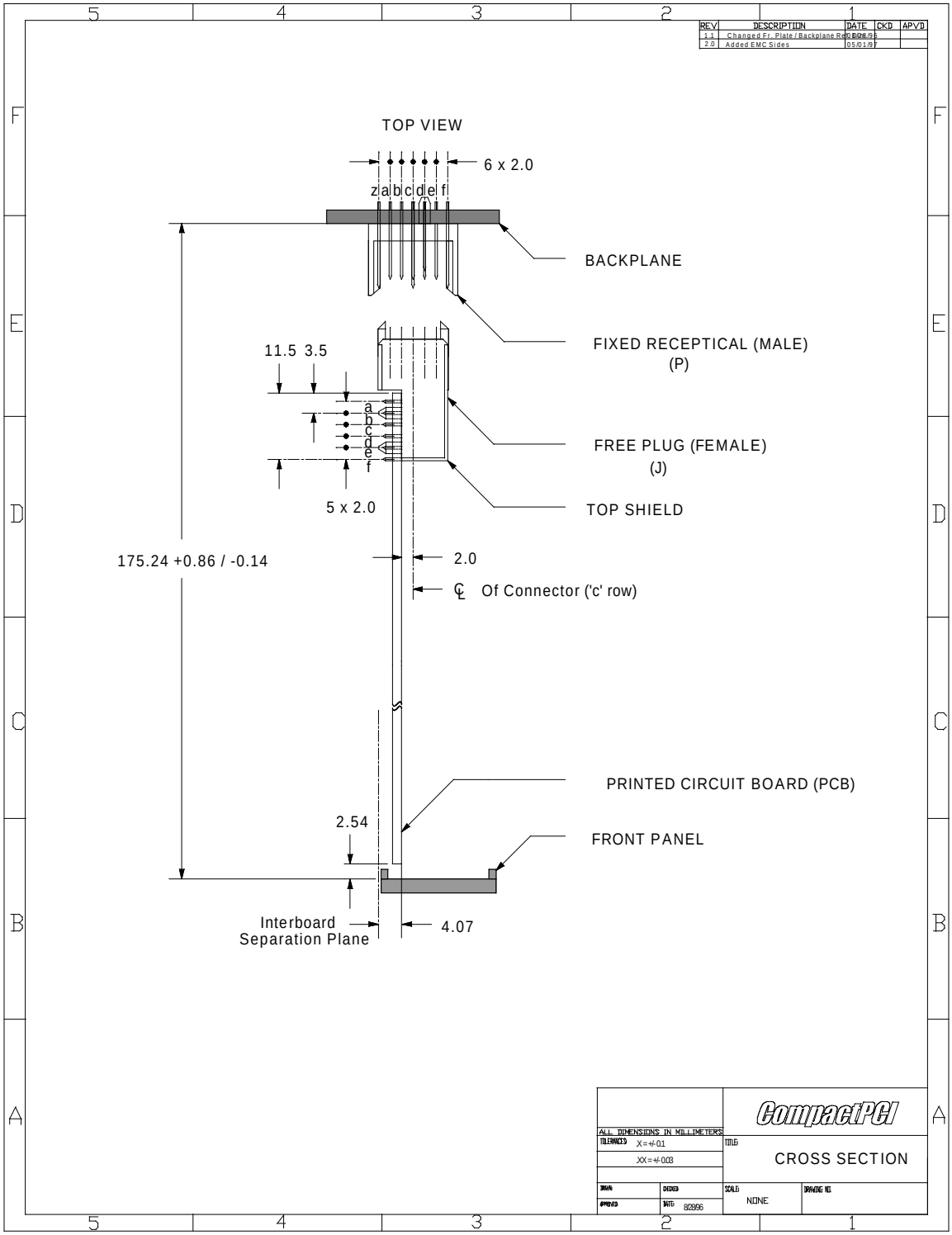


Figure 10. Cross Sectional Board, Connector, Backplane and Front Panel View.

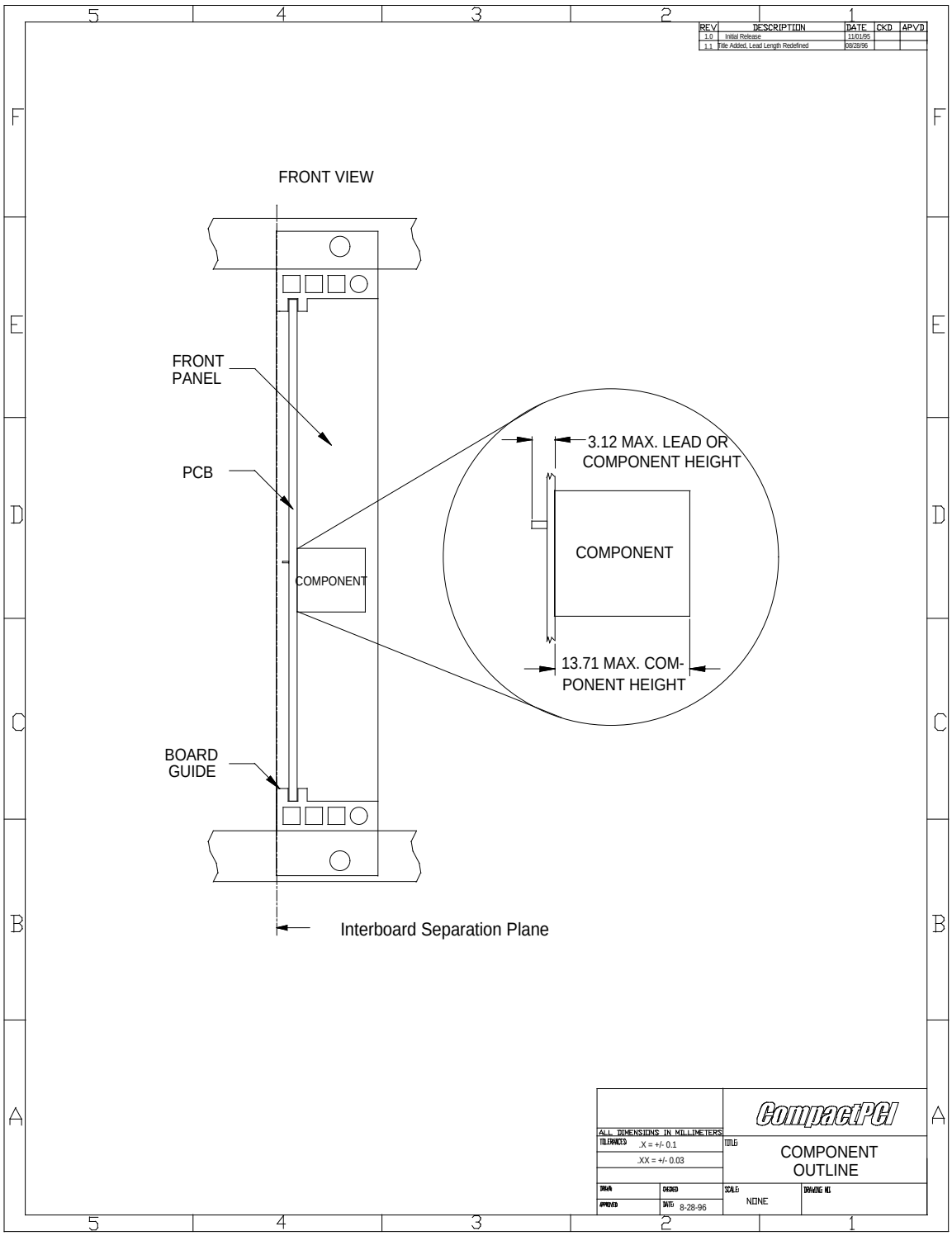


Figure 11. Component Outline.

4.1.4 Front Panels

CompactPCI boards provide a front plate interface that is consistent with Eurocard packaging. CompactPCI boards **shall** use front panels that are compliant with IEEE 1101.1 (for flat panels) or IEEE 1101.10 (EMC panels). IEEE 1101.10 for EMC panels is preferred and **should** be used on all boards and filler panels.

Ejector/injector handles that are compliant with IEEE 1101.10 **shall** also be used. One ejector handle **shall** be used for 3U boards. 6U boards **shall** use two handles. Filler panels do not require handles. Sub-racks **shall** also comply with IEEE 1101.10.

Front entry of CompactPCI boards into the subrack is defined by IEEE 1101.1 and IEEE 1101.10. Rear entry of boards (real panel I/O) into the subrack is defined by IEEE P1101.11.

Physical board locations within the subrack **should** be indicated by a numbering scheme visible from the front (and rear if back panel I/O is utilized) of the subrack. Physical numbers **should** be placed within the compatibility glyphs.

Connector cutouts, labeling, and handle appearance may vary as required. The CompactPCI logo **shall** be clearly visible on the front panel.

Board compatibility glyphs **shall** be displayed on the front panel. Capability glyphs are:

- △ (triangle) for System Slot
- ○ (circle) for Peripheral Slots

Figure 12 illustrates the CompactPCI compatibility glyphs. Boards that can be used in either a System Slot or Peripheral Slot **shall** combine both compatibility glyphs on top of one another.

Figure 12. CompactPCI Compatibility Glyphs.

Figure 13 illustrates the CompactPCI logo that **shall** be used on the front panels. The font style is Italic Impact.

CompactPCI™

Figure 13. CompactPCI Logo.

4.1.4.1 3U Front Panels

3U boards **shall** use one IEEE 1101.10 handle located on the bottom as illustrated in Figure 14.

4.1.4.2 6U Front Panels

6U boards **shall** use two IEEE 1101.10 handles as illustrated in Figure 15.

4.1.5 System Slot Identification

System Slot capability **should** be indicated within a CompactPCI subrack by red guide rails. This allows users to easily locate the System Slot.

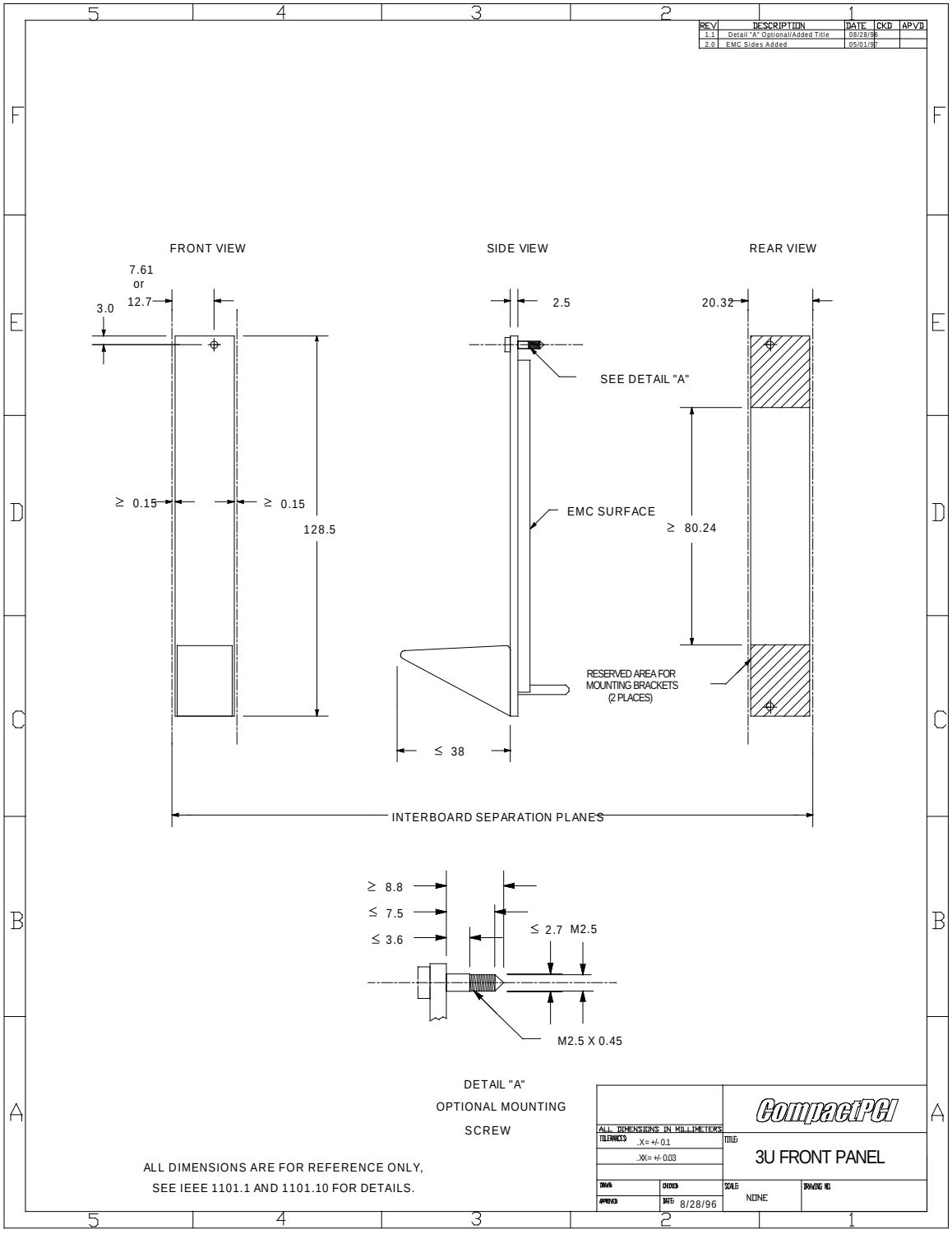


Figure 14. 3U EMC Front Panel.

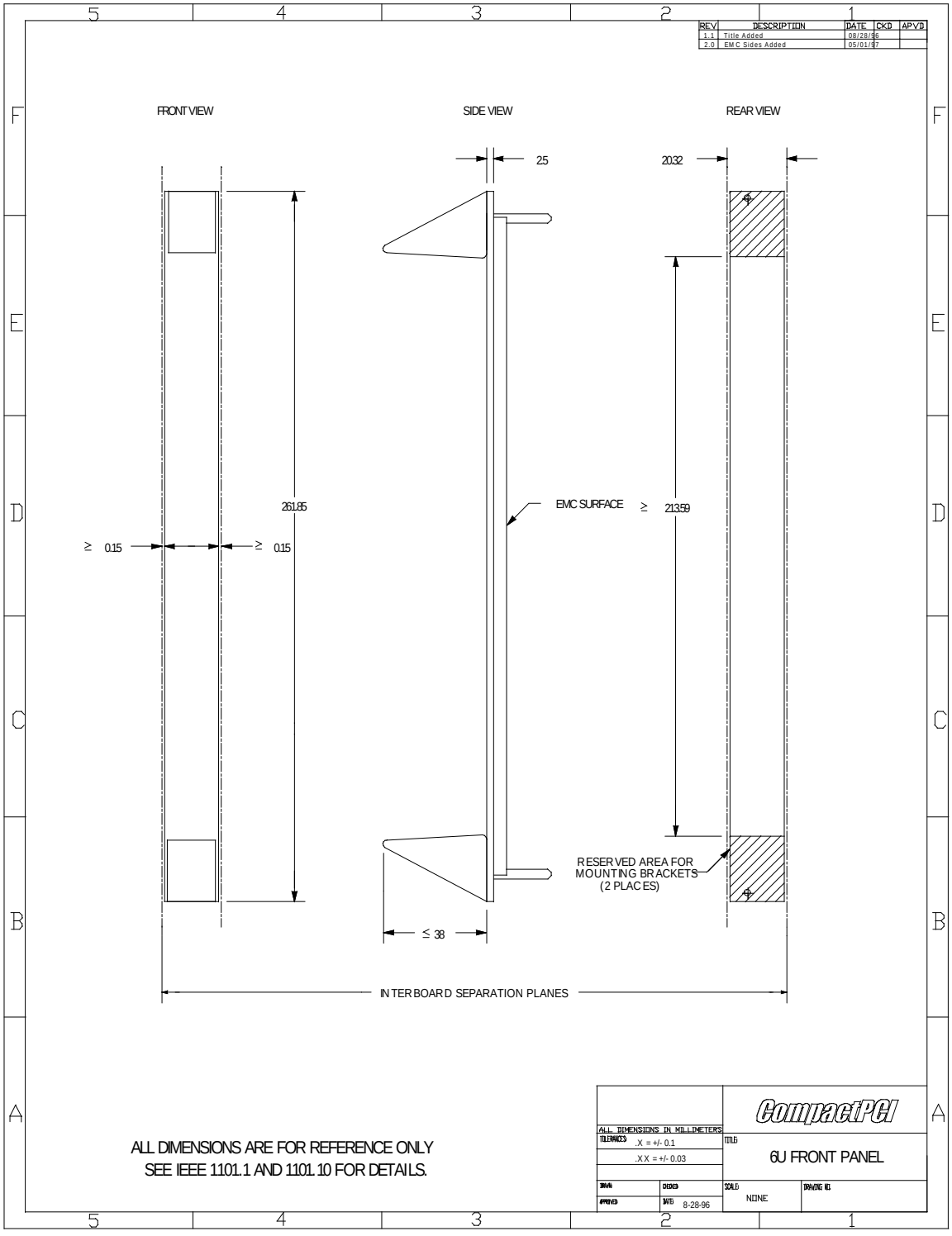


Figure 15. 6U EMC Front Panel.

4.2 Rear-Panel I/O Board Requirements

The front plug-in boards may route I/O through the backplane via the J2/P2, J3/P3, J4/P4 and J5/P5 connector pairs, using any combination of connectors. In many applications, the only practical way to route this I/O off the backplane is to utilize a rear I/O transition board that has standard I/O connectors for each particular type of I/O.

4.2.1 Mechanicals

IEEE Draft Standard P1101.11 defines the generic mechanics for rear-panel I/O transition boards. The mechanical implementation of rear-panel I/O transition boards and subracks **should** be in accordance to IEEE Draft Standard P1101.11 for 80 mm deep boards and subracks (also see Section 4.1.1.3).

The same front panel, the same handles, the same keying, the same alignment pin, the same EMC and the same ESD mechanics **should** be used as on the front CompactPCI boards.

The same subrack rails, card guides, EMC support, ESD support, keying, alignment pin hole, and injector/extractor comb **should** be used as on the subrack front side, except for the card guide's depth.

Note that rear-panel I/O transition boards are "in-line" with the front CompactPCI boards. This means that the front panels of rear-panel I/O transition boards are reversed (mirrored) from the front boards. The top handles are on the bottom and the bottom handles are on the top. The slot keying holes and hole labels in both the card guides and front panels will be upside down as compared to the front boards and card guides.

The same connector pin labeling sequence **should** be used on the rear I/O transition boards as the on front boards, with the position numbers going from bottom to top. Effectively this is a mirror image of the front board’s layout orientation. By using the same 1 for 1 pin mapping labeling sequence eliminates confusion and I/O signal pin mapping problems. Example, pin A3 is the same on the front boards, on the rear I/O transition board and on the backplane.

4.2.2 Power

In some applications, the rear-panel transition board will have active components. Power can be applied either through the I/O pins from the front board, or from the normal power and ground pins defined as part of the J1/P1 and J2/P2 connector pin assignments.

4.3 Backplane Requirements

4.3.1 Connector Orientation

The bus segment connector orientation is illustrated in Figure 16 when viewed from the front of the system chassis. The System Slot **may** be located in any position on a backplane but **shall** be located on either end of the bus segment unless otherwise simulated to ensure compliance to the PCI specification.

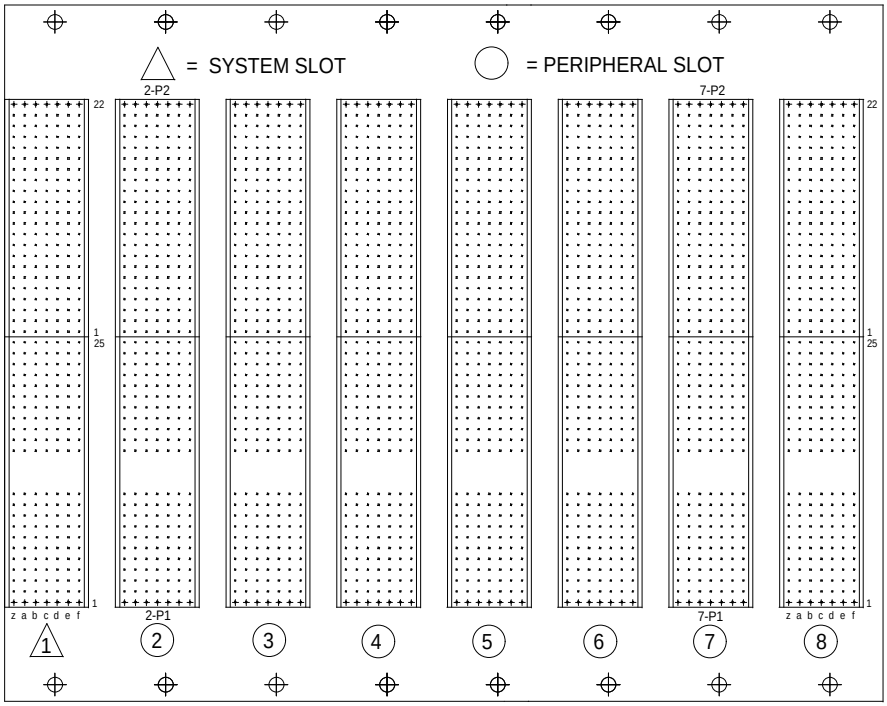


Figure 16. 3U Backplane Example.

4.3.2 Slot Spacing

This specification and all backplane simulations have assumed a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

Bus segments **shall** not have more than eight slots without one or more PCI bridges.

4.3.3 Slot Designation

Physical backplane slots **shall** be designated 1, 2, 3, through N, where N is the number of slots. For example, an eight slot backplane would designate the backplane slots as 1 through 8 with the compatibility glyphs. Slot numbering **shall** start at the top left corner as viewed from the front.

Logical slot numbers **shall** be defined by the IDSEL and associated address used to select the slot as defined in Table 7. Logical slot numbers are used in the nomenclature to define the physical outline of a connector on a bus segment. Please see Chapter 3 for signal routing requirements.

Each slot **may** be implemented with one or more connectors. Backplane connectors **shall** be designated as P1 through P5, corresponding in location to the board's connectors illustrated in Figure 7 and Figure 8.

Any given connector **shall** be referenced by first specifying the logical slot number (1...8) followed by a hyphen and then the individual connector (P1...P5). For example, in a 32-bit 3U system 5-P2 would designate the rear-panel I/O connector in logical slot 5. In a 64-bit 6U system 1-P3 would designate the rear-panel I/O connector in logical slot 1.

4.3.4 Bus Segments

Bus segments **may** accommodate 64-bit operation or **shall** provide individual pull-up resistors at each board slot for the REQ64# and ACK64# signals. Refer to the PCI specification for details. The System Slot **shall** use both J1 and J2 to allow the arbitration and clock signals to be connected to the backplane from a System Slot board. Connectors require pin staging (see Section 5.7) to accommodate hot swap operation.

CompactPCI bus segments **shall** bus all signals in all slots within the segment except the slot specific signals: CLK, REQ# and GNT#. Each logical slot also has a unique IDSEL signal connected to one of the upper ADxx signals for configuration (plug and play) decoding.

Backplanes implementing the modular power supply connector **shall** provide connection for the power supply signals DEG#(P2:C16) and FAL# (P2:C15) at the System Slot that may be provided by the power supply.

4.3.5 Backplane Dimensions

Depending on system design requirements, termination networks, etc., the left and right ends of a backplane can be made longer. Whenever extended, the end dimensions **shall** be in increments of 5.08 mm. This will allow for modular construction of backplanes and subracks.

4.3.5.1 3U Backplanes

A 3U backplane without a power connector is illustrated in Figure 17. Figure 18 illustrates a 3U backplane with a power connector. Both figures illustrate physical slot locations designated 1 through 8.

4.3.5.2 6U Backplanes

A 6U backplane without a power connector is illustrated in Figure 19. Physical slot locations are designated 1 through 8.

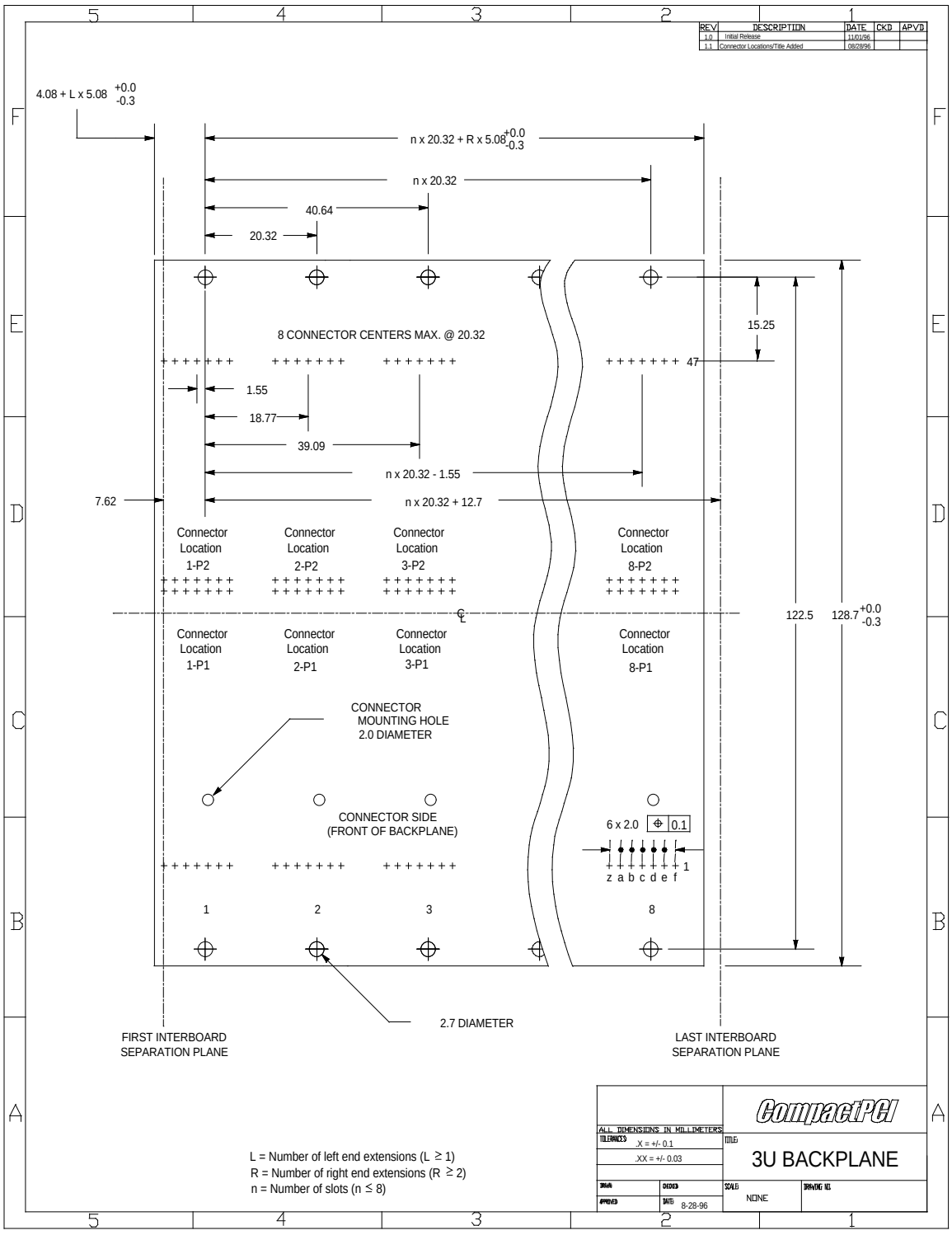


Figure 17. 3U Backplane Dimensions.

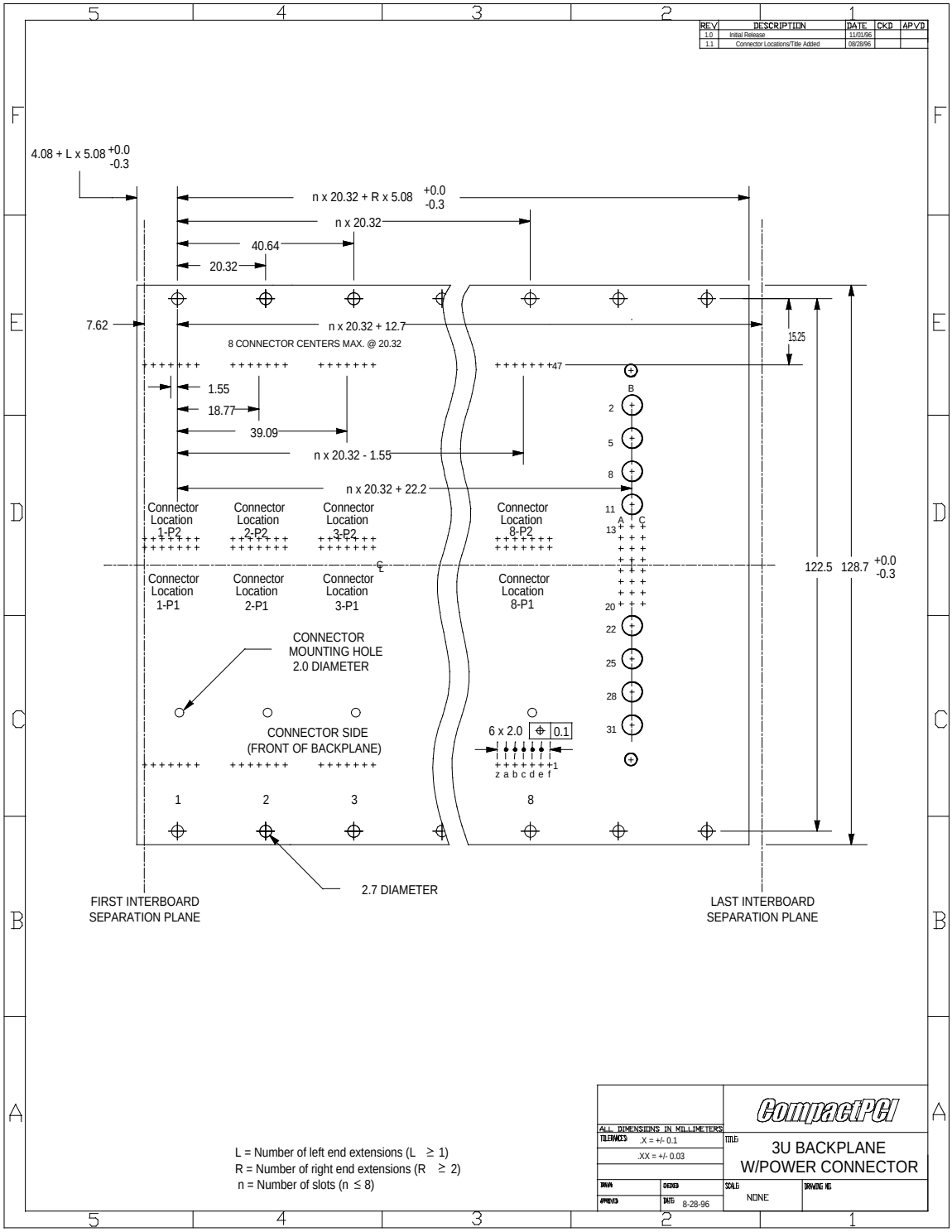


Figure 18. 3U Backplane Dimensions with Power Connector.

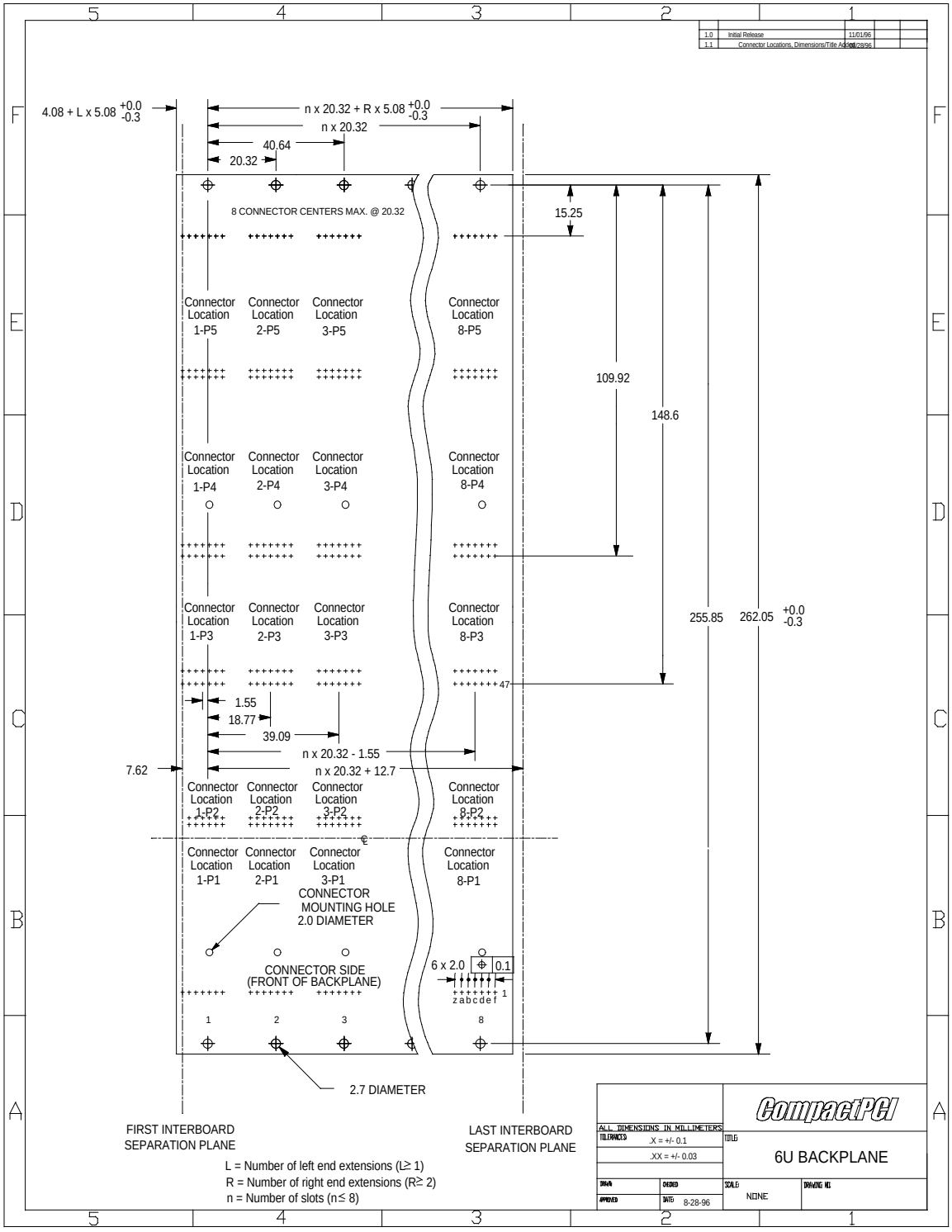


Figure 19. 6U Backplane Dimensions.

5. Connector Implementation

5.1 J1 (32-Bit PCI Signals)

CompactPCI board connector J1 is used for the 32-bit PCI signals as illustrated in Table 14. 32-bit boards **shall** always use this connector. Use of the J2 connector is optional.

5.2 J2 Connector

J2 **may** be used for 64-bit PCI transfers or for rear-panel I/O. The keying of this connector function is provided by the IEEE 1101.10 front panel key. J2 **shall** be used on System Slot boards to provide arbitration and clock signals for peripheral boards. J2 **shall** be used if 64-bit PCI operation, rear-panel I/O, or geographic addressing is supported.

5.2.1 64-Bit PCI

The mapping of 64-bit PCI within J2 is shown in Table 14.

5.2.2 Rear-Panel I/O

The mapping of rear-panel I/O within J2 is shown in Table 15.

5.3 Bussed Reserved Pins

The BRSVPxxx signals **shall** be bussed between connectors and are reserved for future definition.

5.4 Non-Bussed Reserved Pins

The RSV signals are non-bussed signals that **shall** be reserved for future definition.

5.5 Power Pins

All CompactPCI connectors provide pins for +5V, +3.3V, +12V and -12V operating power. Additional power pins labeled +V(I/O) provide power for Universal boards utilizing I/O buffers driving backplane signals that **may** operate from +5V or +3.3V. On these boards, the PCI component's I/O buffers shall be powered from V(I/O), not from +5V or +3.3V power pins.

Backplane pins labeled V(I/O) are connected to +5V on 5 V keyed systems and +3.3V on 3.3 V keyed systems. Alternatively, a separate V(I/O) power plane may be provided to supply 5 V or 3.3 V power.

The IEC 1076-4-101 connector is a press-fit connector. Connections between the voltage planes and connector pins should be a solid (no thermal relief) interconnect. This provides a low inductance connection between the connector pin and each power plane.

5.6 5V/3.3V PCI Keying

CompactPCI implements a keying mechanism to differentiate 5 V or 3.3 V signaling operation. The keying mechanism is designed to prevent a board built with one buffer technology (5 V or 3.3 V) from being inserted into a system designed for the other buffer technology (3.3 V or 5 V, respectively). Universal boards **may** operate in either +5V or +3.3V systems and are not keyed. Positions 12-14 of the CompactPCI connector are used for the keying mechanism. Backplanes **shall** be configured as either 5V or 3.3V and **shall** provide the appropriate key. It is not possible to have a "universal" backplane. Refer to the *CompactPCI Keying Specification* for additional details on keying.

Table 13. Coding Key Color Assignments and Part Numbers.

Signaling Voltage V(I/O)	**Color Reference**		**Code #**	
	Color	**RAL # (1)**	**Male (Backplane)**	**Female (Board)**
3.3 V	Cadmium Yellow	1021	3456	1278
5 V	Brilliant Blue	5007	1567	2348
3.3 V or 5 V (Universal Board)	-	-	N/A(2)	No Key

Notes:

1. RAL is a trademark of the central organization for product assurance in Germany. One of its tasks is harmonization in the use of colors. Color samples may be ordered from: Muster-Schmidt KG, RAL - Farbkartenvertrieb, Postfach 2751, D - 3400 Gottingen, Germany.
2. Backplanes **shall** be configured for either 5 V or 3.3 V V(I/O). Plug in boards may be designed to be universal and **shall** therefore have no key loaded.

5.7 Pin Assignments

Table 14. CompactPCI 64-Bit Connector Pin Assignments[(1)(10, 11)].

22	GND	GA4[(13)]	GA3[(13)]	GA2[(13)]	GA1[(13)]	GA0[(13)]	GND	
21	GND	CLK6[(3) (16)]	GND[(3) (16)]	RSV	RSV	RSV	GND	
20	GND	CLK5[(3) (16)]	GND[(3) (16)]	RSV	GND[(15)]	RSV	GND	
19	GND	GND[(3) (16)]	GND[(3) (16)]	RSV	RSV	RSV	GND	P2
18	GND	BRSVP2A18[(12)]	BRSVP2B18[(12)]	BRSVP2C18[(12)]	GND[(15)]	BRSVP2E18	GND	/
17	GND	BRSVP2A17[(12)]	GND[(15)]	PRST#[(3)]	REQ6#[(3) (8)]	GNT6# [(3) (8)]	GND	J2
16	GND	BRSVP2A16[(12)]	BRSVP2B16[(12)]	DEG#[(3)]	GND[(15)]	BRSVP2E16	GND	
15	GND	BRSVP2A15[(12)]	GND[(15)]	FAL#[(3)]	REQ5#[(3) (8)]	GNT5# [(3) (8)]	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)[(2)]	AD[37]	AD[36]	GND	C
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	O
11	GND	AD[45]	GND	V(I/O)[(2)]	AD[44]	AD[43]	GND	N
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	N
9	GND	AD[52]	GND	V(I/O)[(2)]	AD[51]	AD[50]	GND	E
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	C
7	GND	AD[59]	GND	V(I/O)[(2)]	AD[58]	AD[57]	GND	T
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	O
5	GND	C/BE[5]#	GND	V(I/O)[(2)]	C/BE[4]#	PAR64	GND	R
4	GND	V(I/O)[(2)]	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND	
3[(3)]	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2[(3)]	GND	CLK2	CLK3	SYSEN#[(4)]	GNT2#	REQ3#	GND	
1[(3)]	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)[(2)]	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	P1
21	GND	3.3V	AD[9]	AD[8]	M66EN[(5)]	C/BE[0]#	GND	/
20	GND	AD[12]	GND	V(I/O)[(2)]	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O) [(2),(6)]	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	GND [(7)]	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	R
5	GND	BRSVP1A5[(12)]	BRSVP1B5[(12)]	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4[(12)]	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z[(14)]	A	B	C	D	E	F[(9)]	

Notes: (See next page)

Notes for Table 14, CompactPCI 64-Bit Connector Pin Assignments:

1. This diagram defines the pin assignments from the front of the system chassis. Refer to Chapter 3 for pin assignment differences between the system and board slots. All pins are medium length (level 2) except connector P1 pins C16 and D15, which are long (level 3) and short (level 1), respectively in anticipation of a future hot swap specification. This scheme has not been adopted as the preferred approach, nor are there any guarantees that it will be.
2. The V(I/O) signals are either 5 V or 3.3 V, depending on the system implementation.
3. The following positions in rows 1-3 of connector P2 are implemented only on the System Slot board: A1-3, B2, C1-3, D1-3, and E1-3. Additionally, the following positions in rows 15-17 and 19-21 of connector P2 are also implemented only on the System Slot board: C15, C16, C17, D15, D17, E15, E17, A19, A20, A21, B19, B20 and B21.
4. Connector P2 pin C2 is grounded at the System Slot only. Remaining slots leave C2 unconnected. Boards that use this signal (e.g., CPU boards that may be used in the System Slot or Peripheral Slot) **shall** provide a local pull-up to V(I/O). System Slot only boards should tie this pin directly to the ground plane.
5. Connector P1 pin D21 (M66EN) is defined as GND for 33 MHz backplanes. Use of this signal in future 66 MHz systems will be as a bussed signal to all slots.
6. Connector P1 pin C16 (long, level 3) was originally used for early power to hot swap capable boards for controlling the buffer logic. See Section 2.4 for additional information on hot swap capability.
7. Connector P1 pin D15 (short, level 1) was originally used as a board select for hot swap capable boards. See Section 2.4 for additional information on hot swap capability.
8. System Slot boards **shall** provide a mechanism to connect any of the Peripheral Slots 2-8 that may need arbitration service depending on the board installed.
9. Observation: Some manufacturers of top shields utilize every other ground pin while some use every ground pin. Note, shield connections mate at approximately the same time as medium length signals pins.
10. CompactPCI connector pin numbering is intentionally different from the connector manufacturer's pin numbering. This was done to allow the connectors to start at the bottom of the board and "grow" upward from J1/P1 through J5/P5.
11. P1 and P2 connector tail lengths are defined to be "short" tail connectors with 4.5 mm tails.
12. BRSVPxxx signals accommodate PCI reserved signals. Bus segments **shall** bus these signals even though the PCI specification defines these pins as no connects.
13. GA[4..0] **shall** be used for geographic addressing on the backplane. Each backplane connector in a CompactPCI system has a unique encoding for GA[4..0]. See Section 3.2.8.6 for details.
14. Not used on System Slot or Peripheral boards.
15. Boards designed to CompactPCI Specification revision 1.0 are not required to connect these grounds and may claim compatibility.
16. Note backplane clock routing at the time of adoption of this specification only support clocks CLK0-CLK4. CLK5-CLK6 provided by a System Slot board are left unconnected on the backplane.

Table 15. CompactPCI Back-Panel I/O Connector Pin Assignments[1][3][8, 9].

22	GND	GA4[11]	GA3[11]	GA2[11]	GA1[11]	GA0[11]	GND	
21	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
20	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
19	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	P2
17	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	/
16	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	J2
15	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	C
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	O
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	N
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	N
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	E
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	C
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	T
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	O
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	R
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)[2]	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN[4]	C/BE[0]#	GND	P1
20	GND	AD[12]	GND	V(I/O)[2]	AD[11]	AD[10]	GND	/
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	J1
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O) [2],[5]	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	GND [6]	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	R
5	GND	BRSVP1A5[10]	BRSVP1B5[10]	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4[10]	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z[12]	A	B	C	D	E	F[7]	

Notes: (See next page)

Notes for Table 15, CompactPCI Back-Panel I/O Connector Pin Assignments.

1. This diagram defines the pin assignments from the front of the system chassis. Refer to Chapter 3 for pin assignment differences between the system and board slots. All pins are medium length (level 2) except on connector P1 pins C16 and D15 that are long (level 3) and short (level 1), respectively in anticipation of a future hot swap specification. This scheme has not been adopted as the preferred approach, nor are there any guarantees that it will be.
2. The V(I/O) signals are either 5 V or 3.3 V, depending on the system implementation.
3. These pin assignments are for Peripheral Boards only. System Slot boards **shall** use the 64-bit pin assignments (see Table 14) for support of the arbitration and clock driving signals.
4. Connector P1 pin D21 (M66EN) is defined as GND for 33 MHz backplanes. Use of this signal in future 66 MHz systems will be as a bussed signal to all slots.
5. Connector P1 pin C16 (long, level 3) was originally used for early power to hot swap capable boards for controlling the buffer logic. See Section 2.4 for additional information on hot swap capability.
6. Connector P1 pin D15 (short, level 1) is used as a board select for hot swap capable boards. See Section 2.4 for additional information on hot swap capability.
7. Observation: Some manufacturers of top shields utilize every other ground pin while some use every ground pin. Note, shield connections mate at approximately the same time as medium length signals pins.
8. CompactPCI connector pin numbering is intentionally different from the connector manufacturer's pin numbering. This was done to maintain consistency with many other existing Eurocard specifications.
9. P1 connector tail lengths are defined to be "short" tail connectors with 4.5 mm tails. P2 **should** use "long" tail connectors with 16.0 mm tails. The 16.0 mm tails are compatible with IEEE P1101.11 for rear plug in boards.

   If P2 is used for bussing (e.g., TDM bus) "short" tails **shall** be used.
10. BRSVPxxx signals accommodate PCI reserved. Bus segments **shall** bus these signals even though the PCI specification defines these pins as no connects.
11. GA[4..0] **may** be used for geographic addressing or back-panel I/O. See Section 3.2.8.6 for details.
12. Not used on System Slot or Peripheral boards.

6. Revision History

This chapter documents the changes made to the CompactPCI Specification.

Table 16. Revision History.

Revision	Date	Description
1.0	November 1, 1995	Initial release
2.0 R2.1	June 17, 1997	Version 2.0 Release 2.1